

MS-7B89 Ver: 1.1

CPU:

AMD AM4

System Chipset:

Promontory B450

(Value DIY or System Builder)

Main Memory:

DDR IV * 4 MAX 64GB

VRM

RI8894 4+2

On Board Chipset:

LPC Super IO -- NCT6795D

LAN RTL8111H

Azalia CODEC - Realtek ALC892

Expansion Slots:

From CPU

PCI Express X16 Slot * 1

From FCH

PCI Express X1 Slot * 1

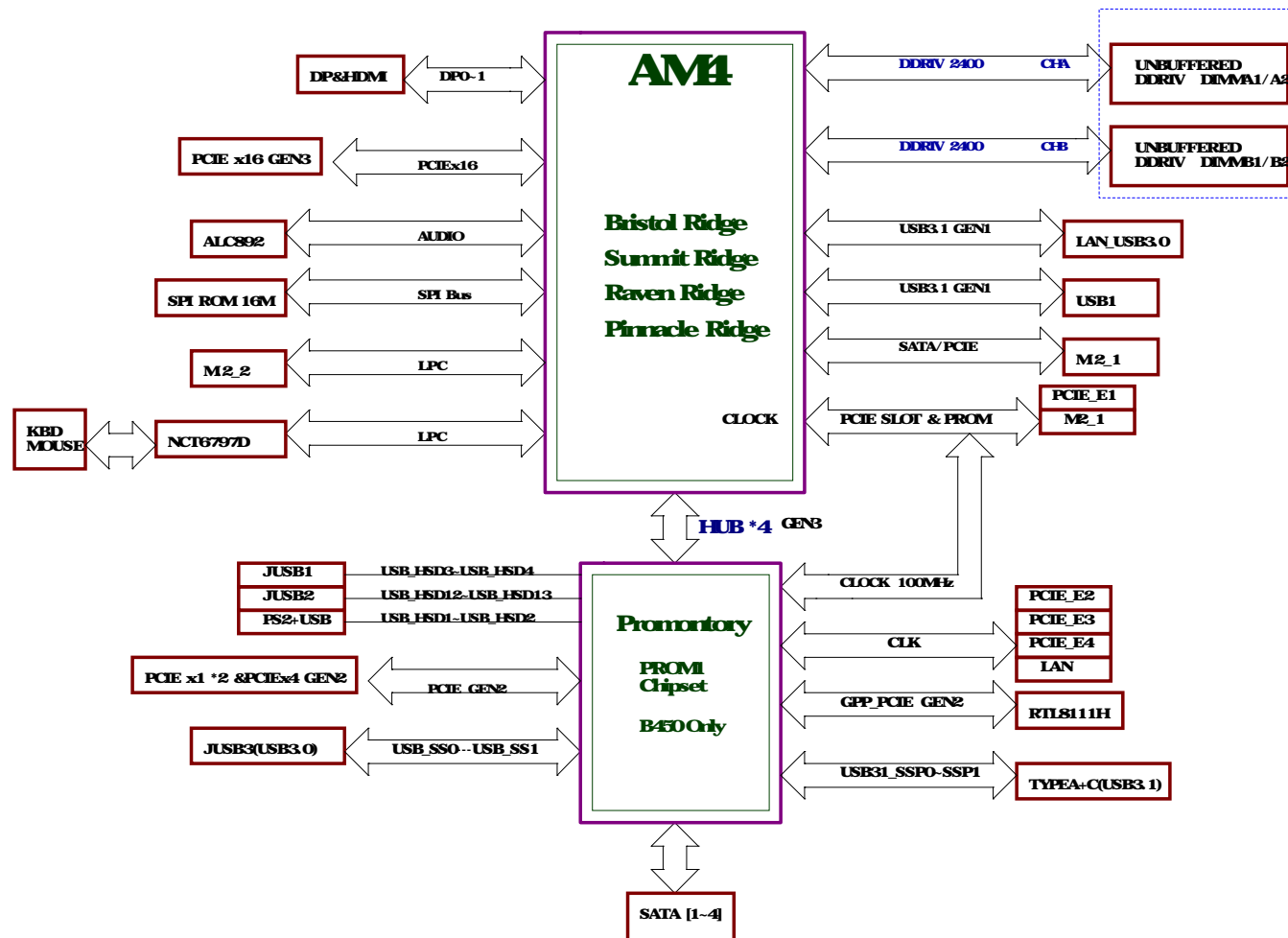
PCI Express X1 Slot * 1

PCI Express X1 Slot * 4

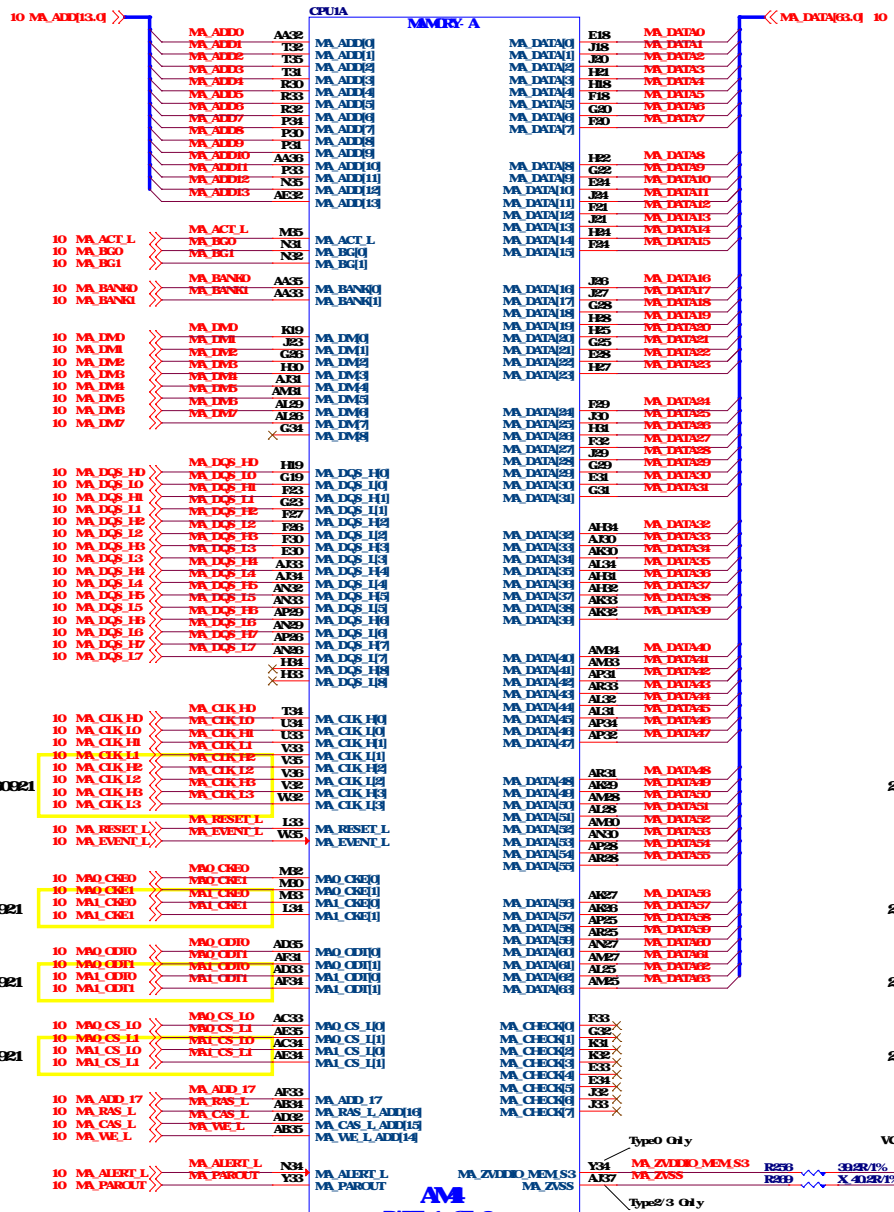
OCF IC:

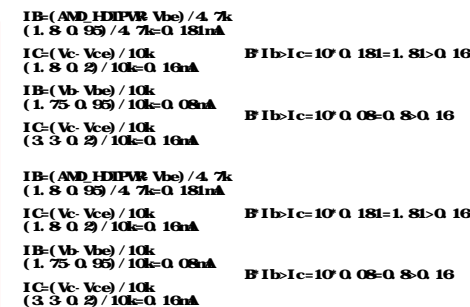
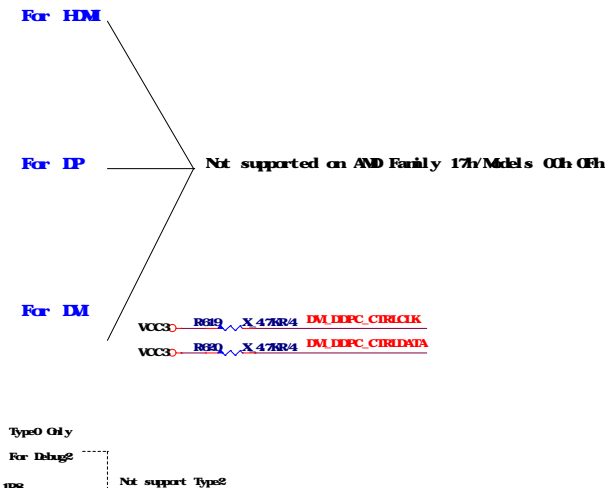
RI9553B

FUSION BLOCK DIAGRAM

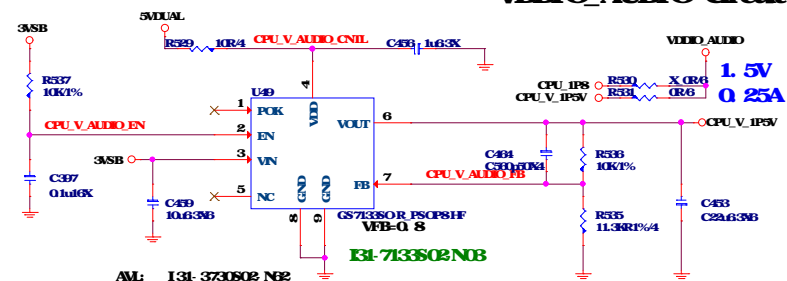


01 Block Diagram	31 Rear USB3.1 TYPE C
02 Cover Sheet	32 USB Front Side
03 AM4 DDR4 IF	33 USB Front JUSB4
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06 AM4 SV/ACPI/GPIO	36 DP
07 AM4 IPC/SPI/USB/CLK/STRAP	37 DMI Connector
08 AM4 Power/RTC Power	38 HDMI
09 AM4 GND	39 ACPI uPI 5V DIMM R3/USB
10 DDR4 DIMMCHA	40 PMNB671GD 1.05V/GS7133 2.5V
11 DDR4 DIMMCHB	41 DDR PWR VPP25V/TT_DDR
12 DDR4 POWER/GND 1	42 DDR4 S125E Power
13 DDR4 POWER/GND 2	43 CPU Power IP8V/MP2147
14 Promontory PCIe/SATA/SATAE	44 CPU Power VDDP-RTS125E
15 Promontory USB/OC	45 CPU Power Connector/PWRGD
16 Promontory CLK/ACPI/GPIO	46 CPU Power RT8804 4+2 Phase
17 Promontory Power	47 CPU Power Phase 1-3
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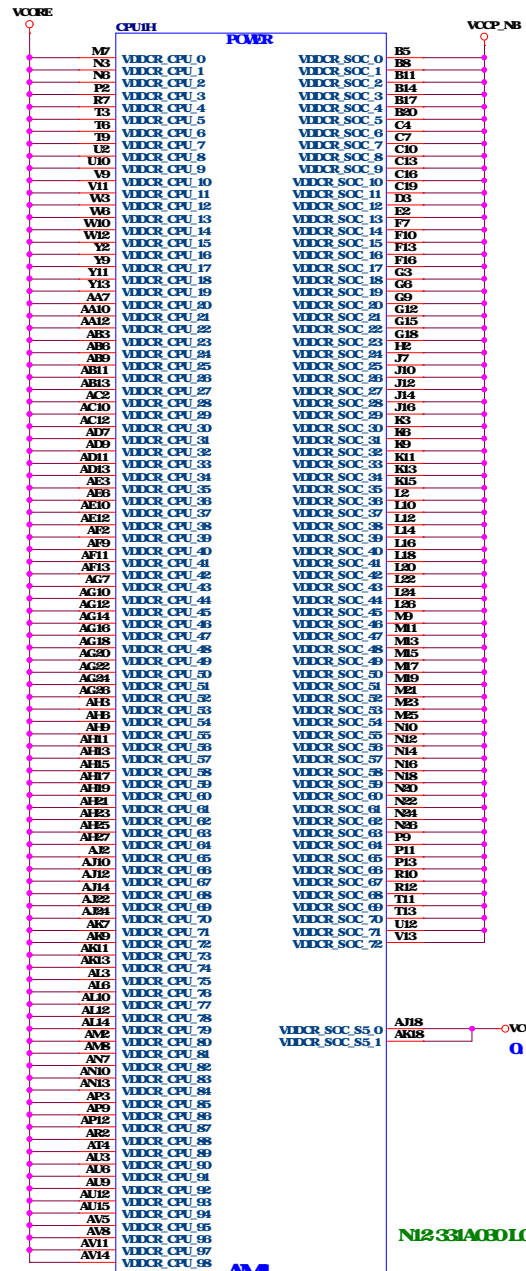
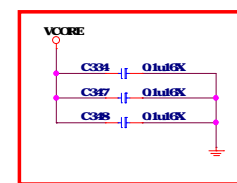


VDIO_AUDIO Circuit



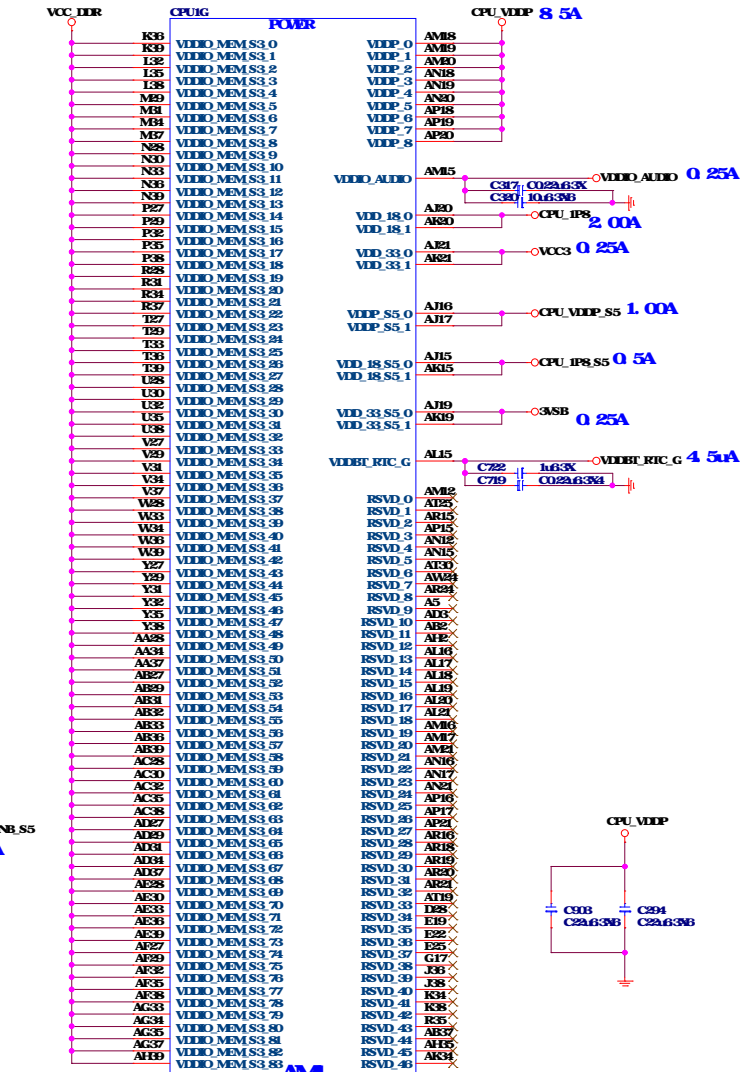
AML: 131-379002 N62

K3-713302 N63



AML PART 8 OF 9

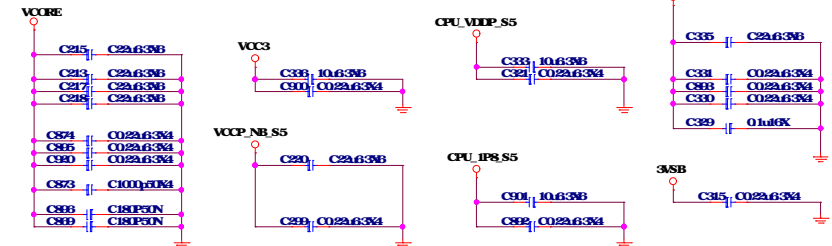
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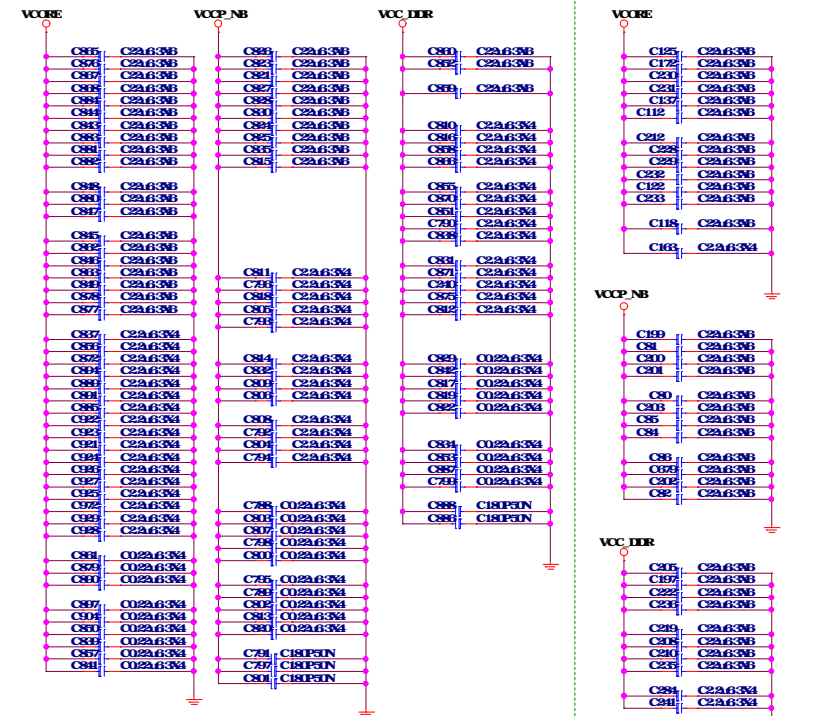
AML PART 7 OF 9

ZIF SOCKET333 HF

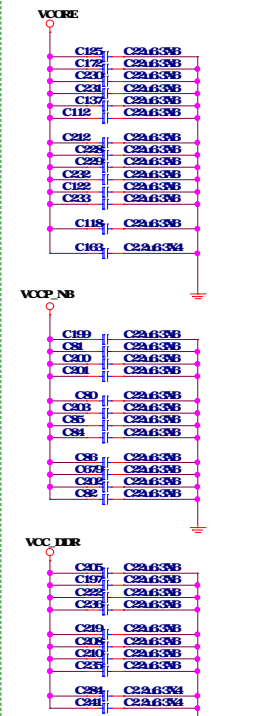
TOP SIDE

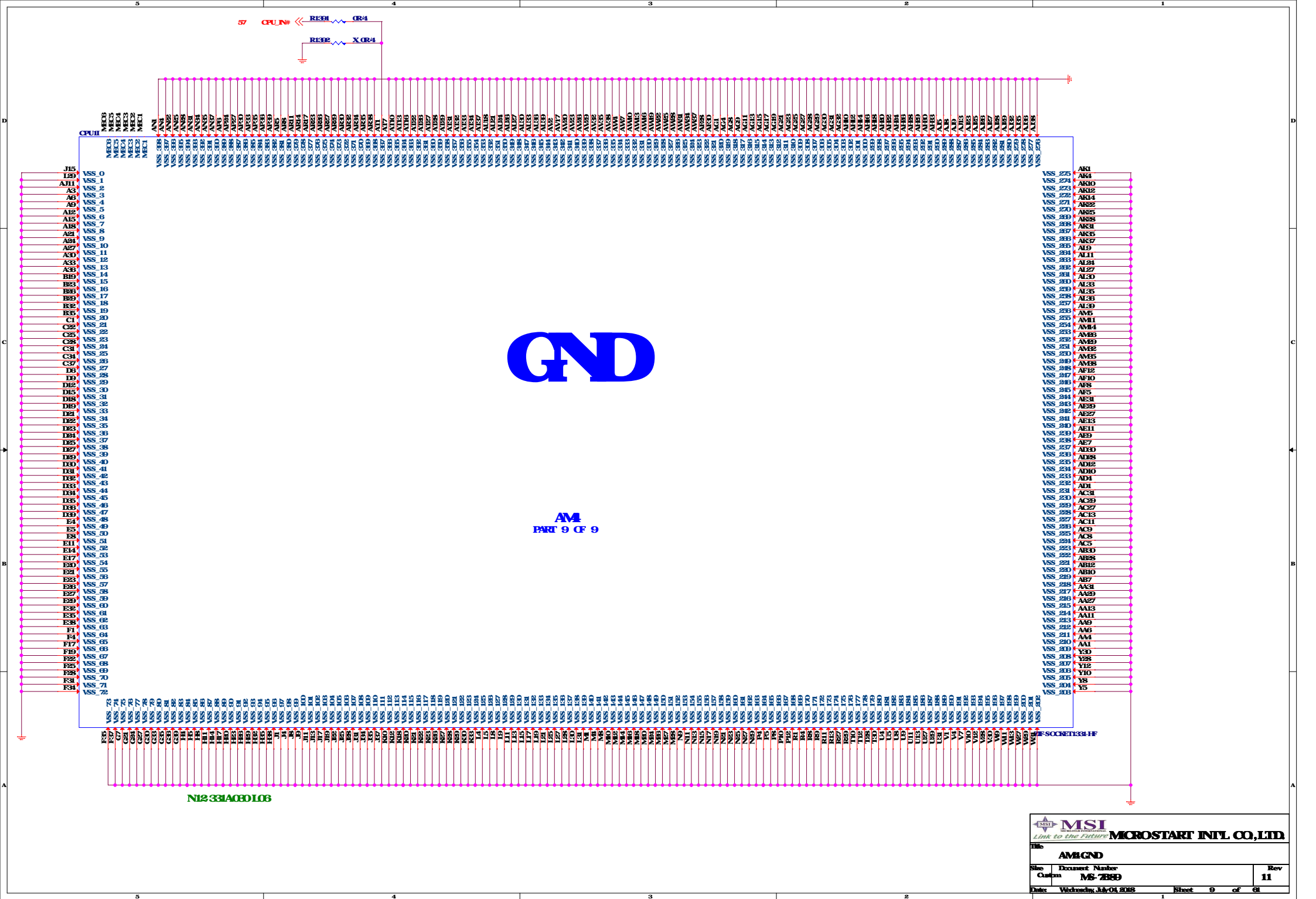


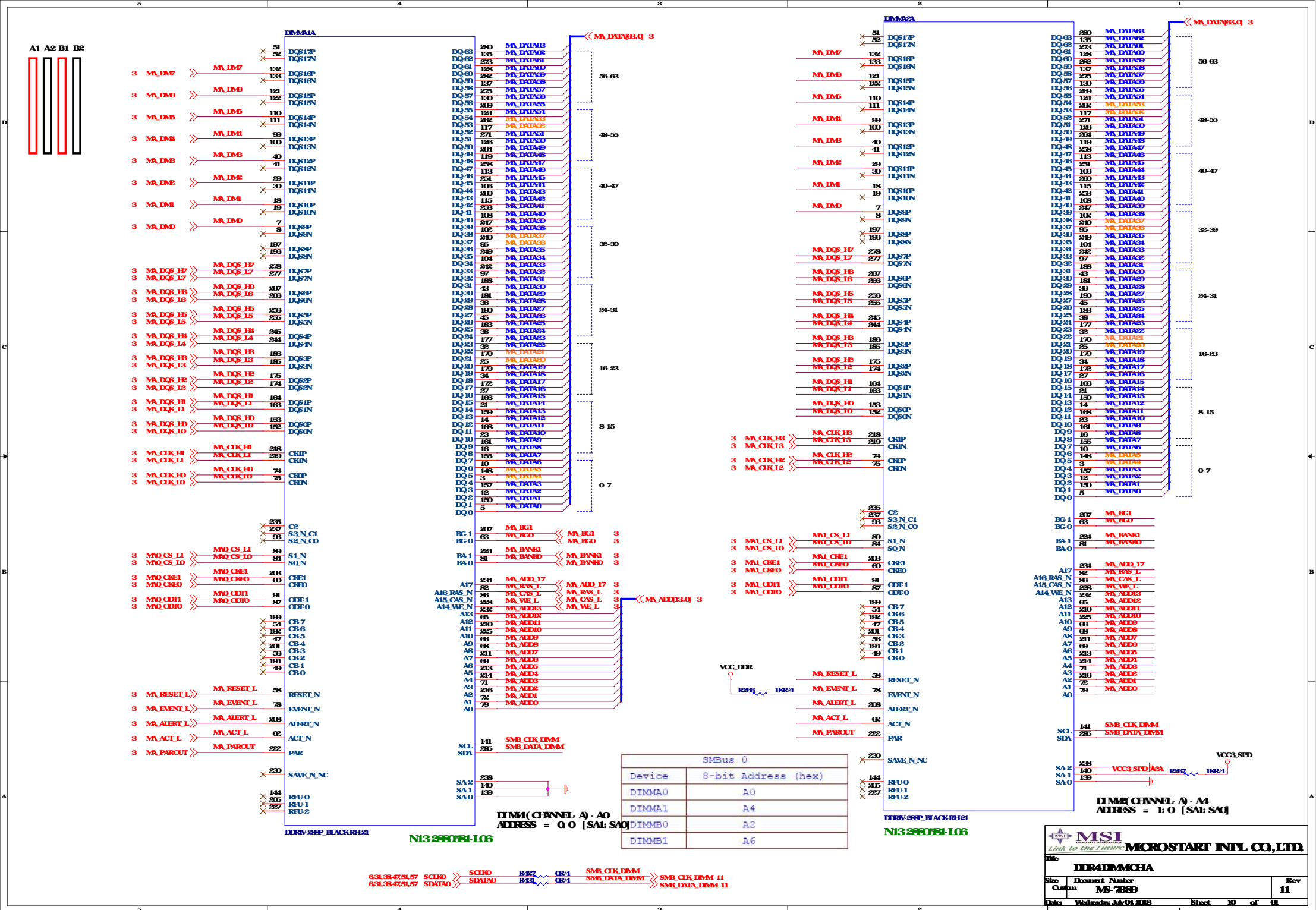
BOTTOM SIDE

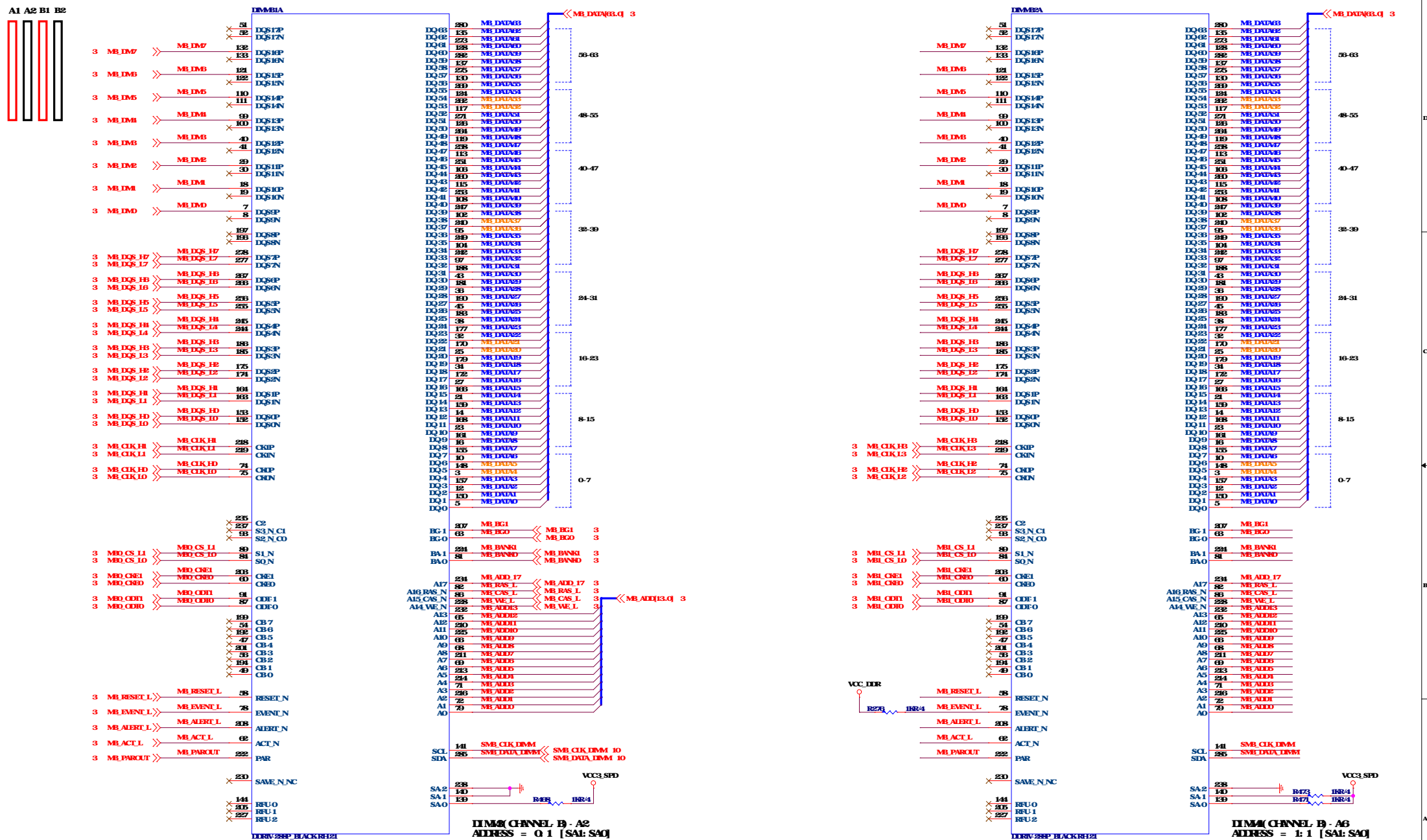


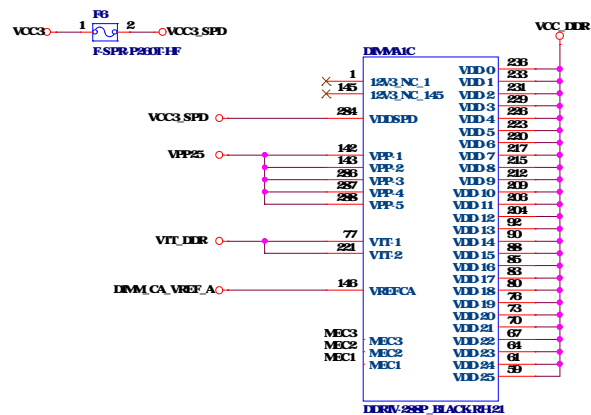
TOP CAVITY



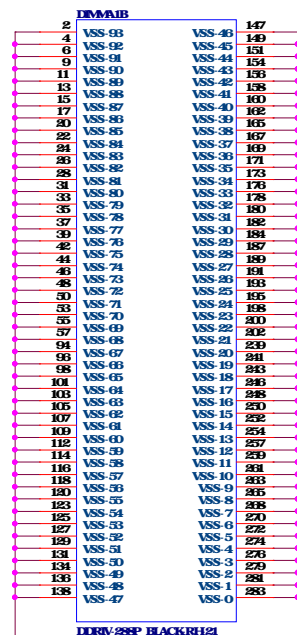
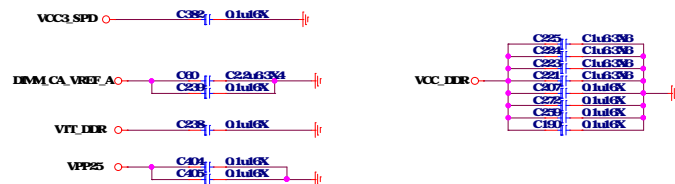






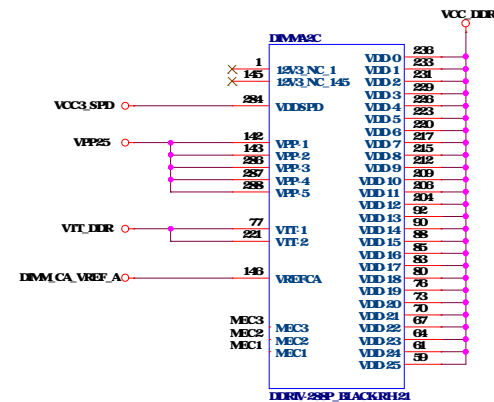


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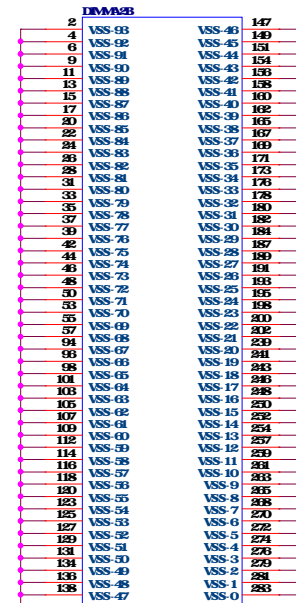
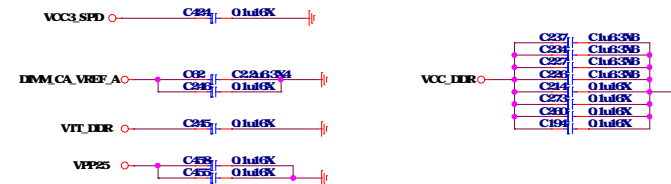


N13 2880581-L06

DIMMSLOT PN BY SPEC



N13 2880581-L06

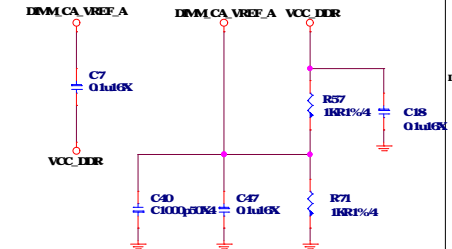


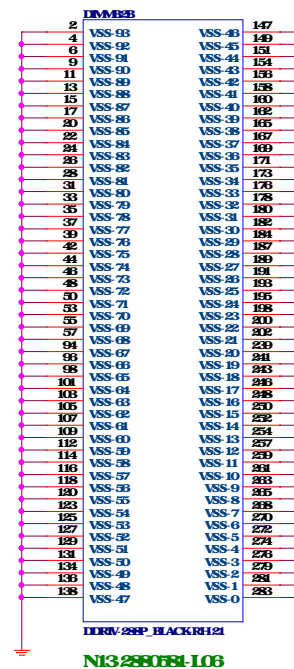
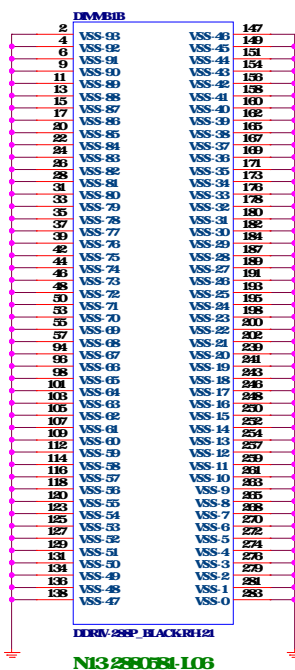
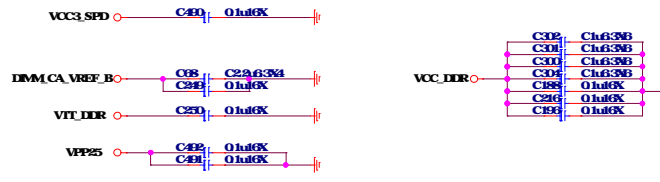
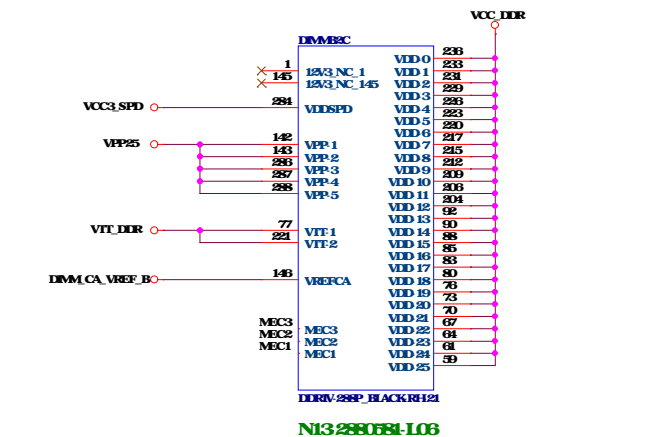
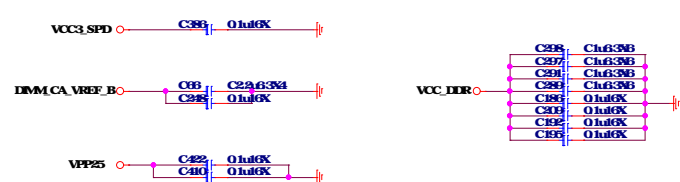
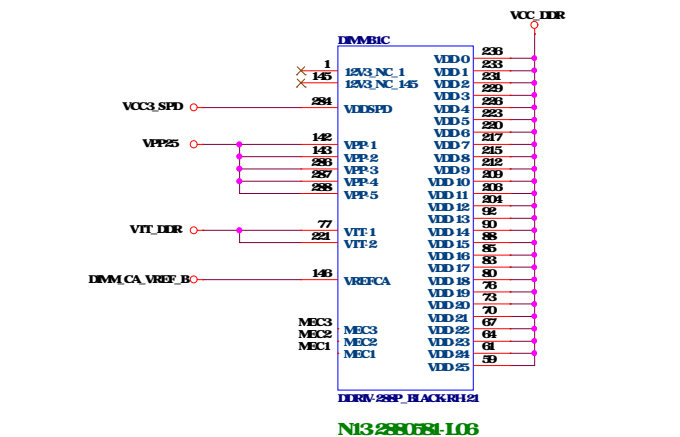
DDRIV-288P_BLACKRH2

N13 2880581-L06

DDR VREF

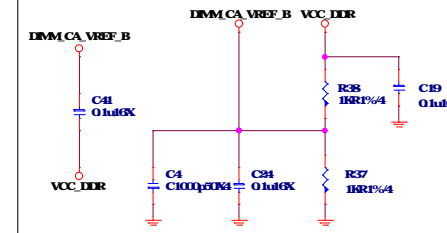
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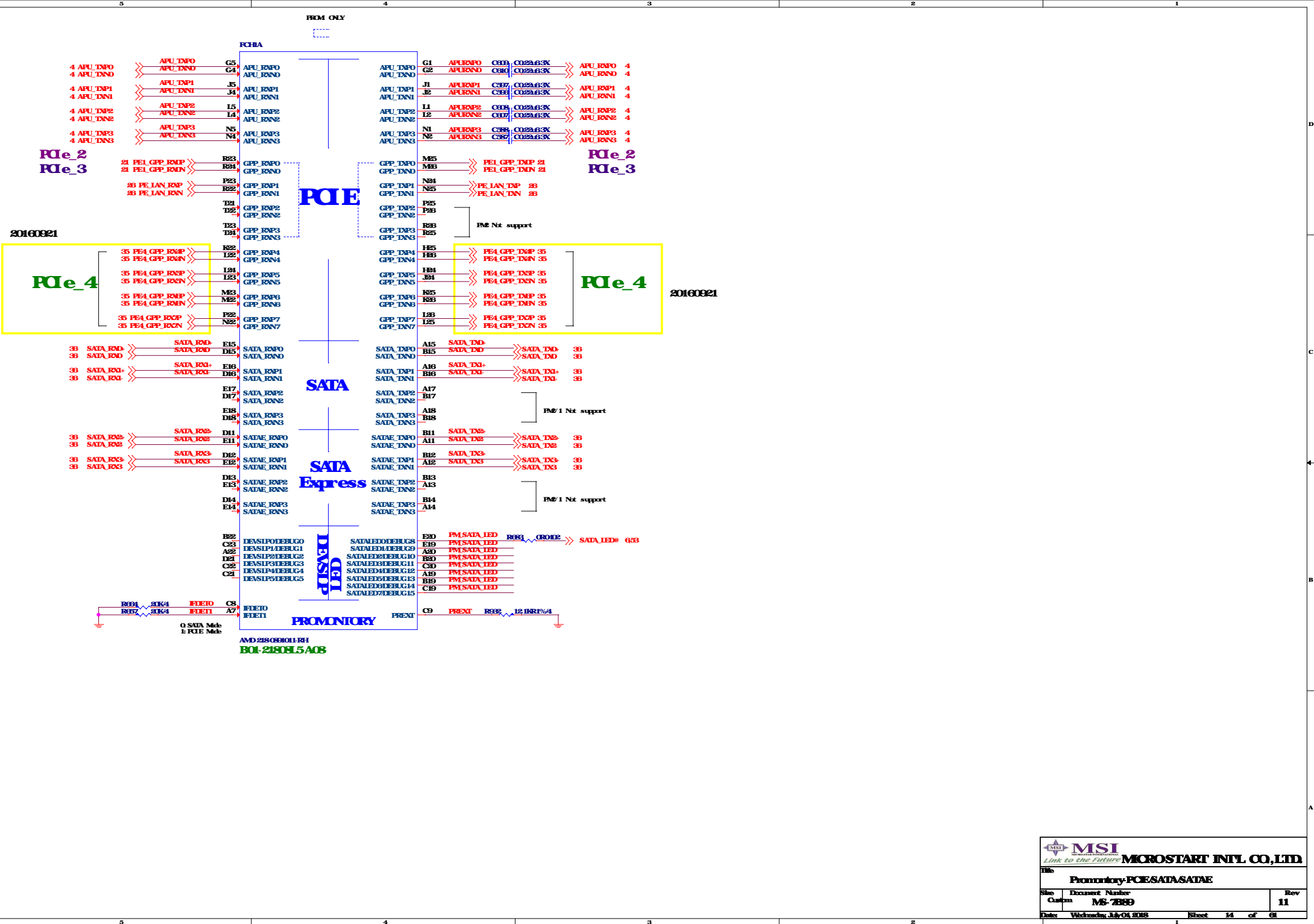


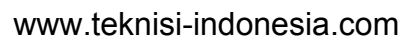


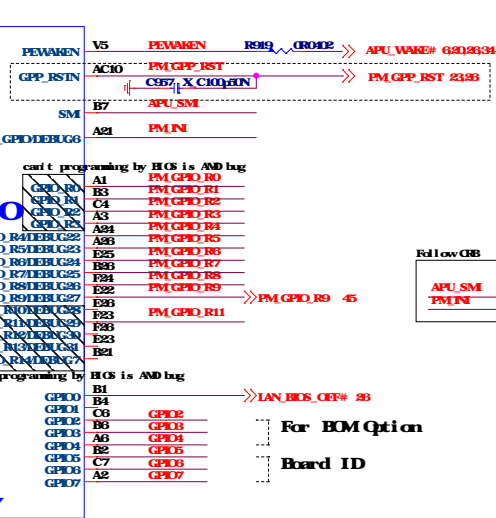
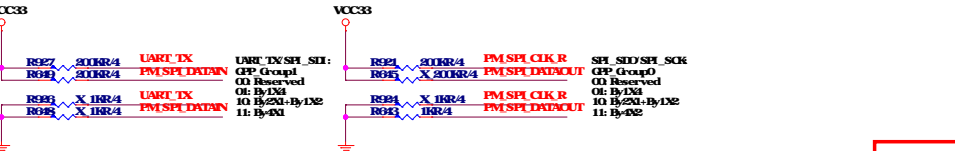
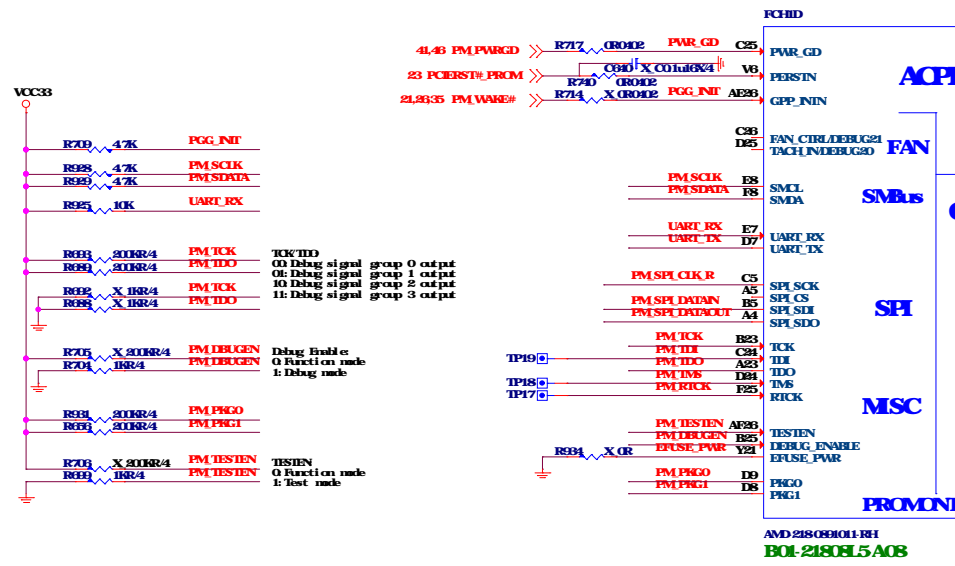
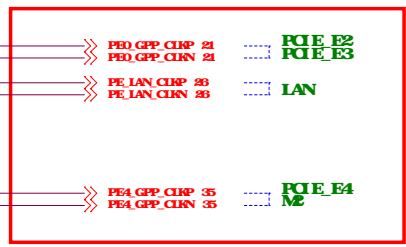
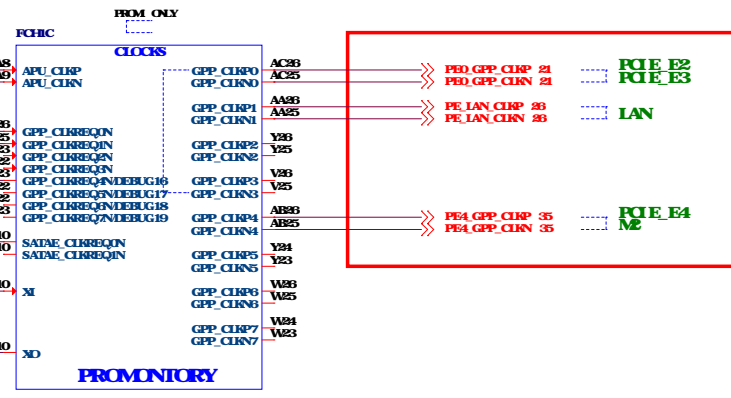
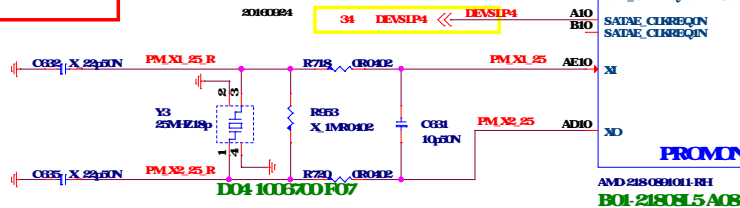
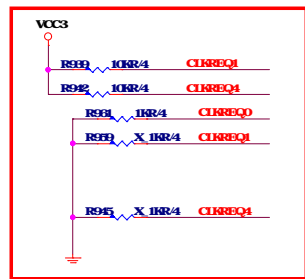
DDR VREF

(place resistors close to DIMMs)

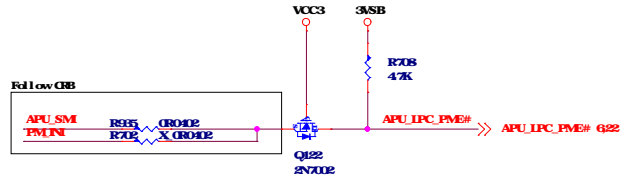








Go lay GPP_RST Reset for next FCH sequence. See 555533



BOMOPTION

	FULL	
GPIOE	0	
GPIOB	0	
GPIOD	0	

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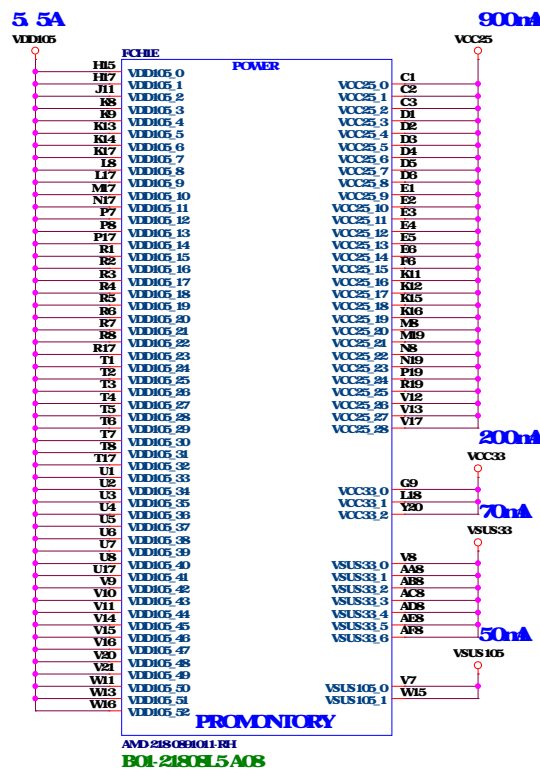
Link to the future

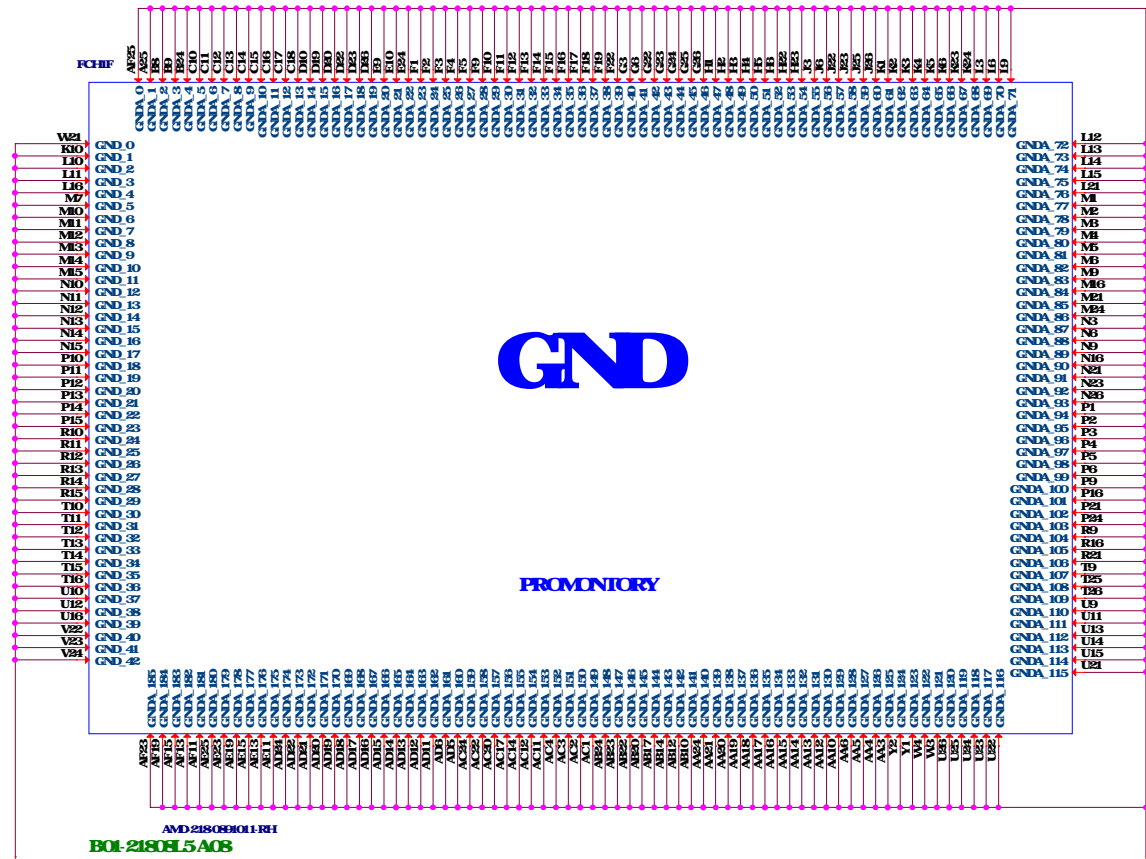
Document Number: MS-7889

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Date: Wednesday, July 04, 2006

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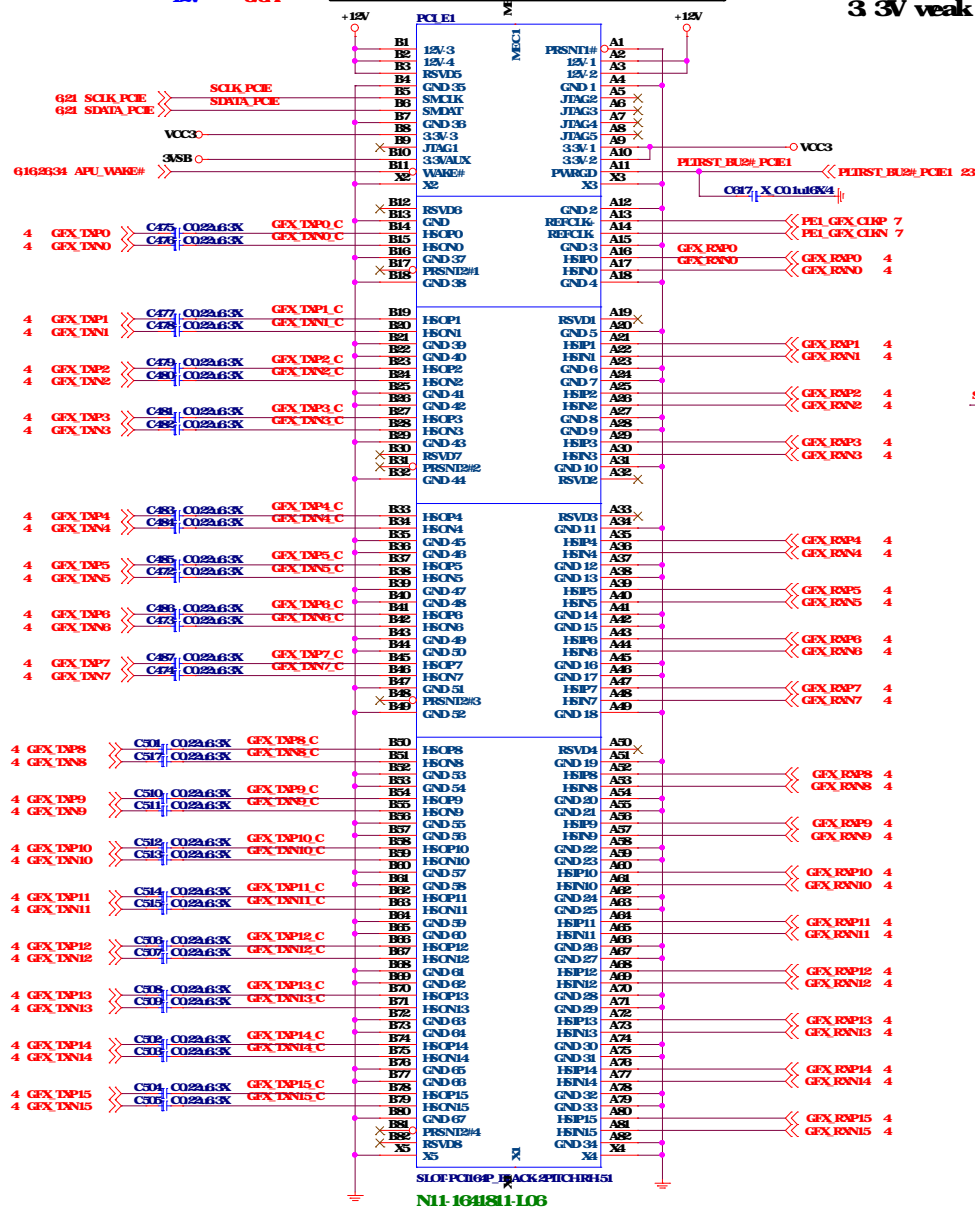
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 MSI <small>Microstart International</small> <i>Link to the Future</i>			MICROSTART INFL CO., LTD.		
Title					
PCE CLK					
Size	Document Number				Rev
Custom	MS-7889				11
Date		Wednesday, July 04, 2005		Sheet	89 of 98

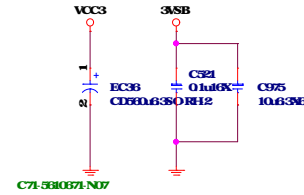
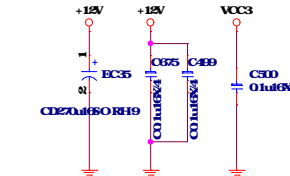
3.3V 30A
12V 5.5A

PCI EXPRESS x16 Slot

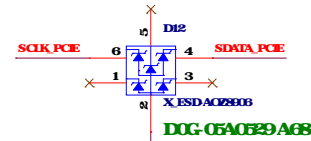
PCIEX1 12V 0.5A
3.3V weak 375mA



C7A-2711701-N07

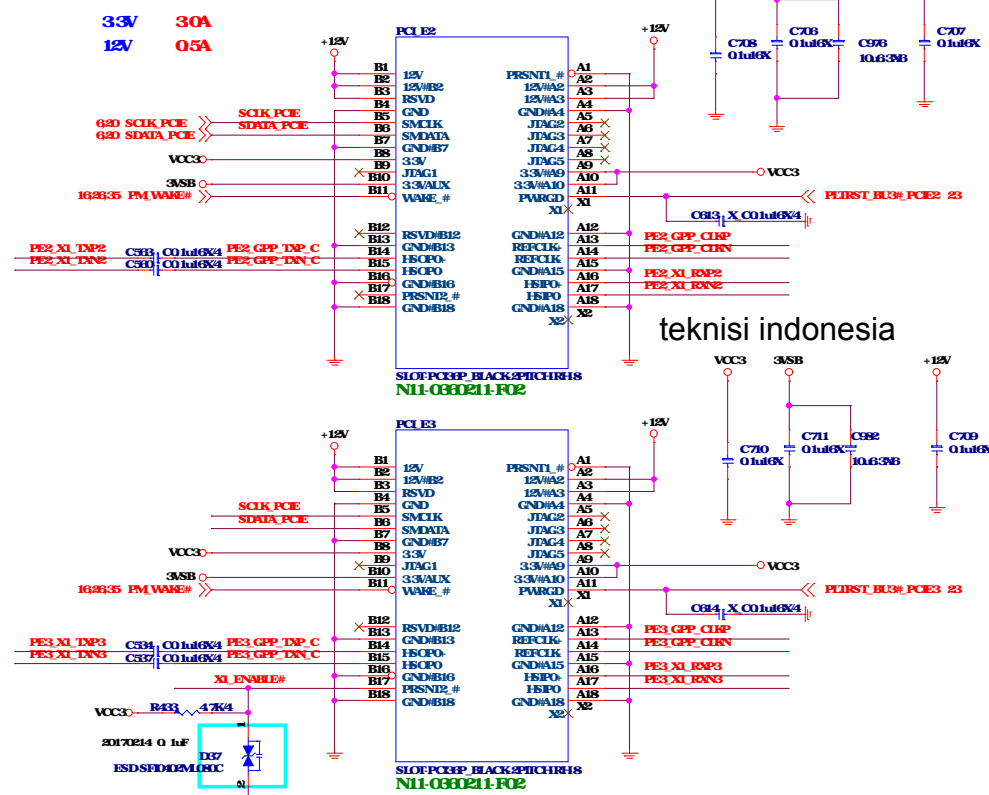


SMBus separate circuit

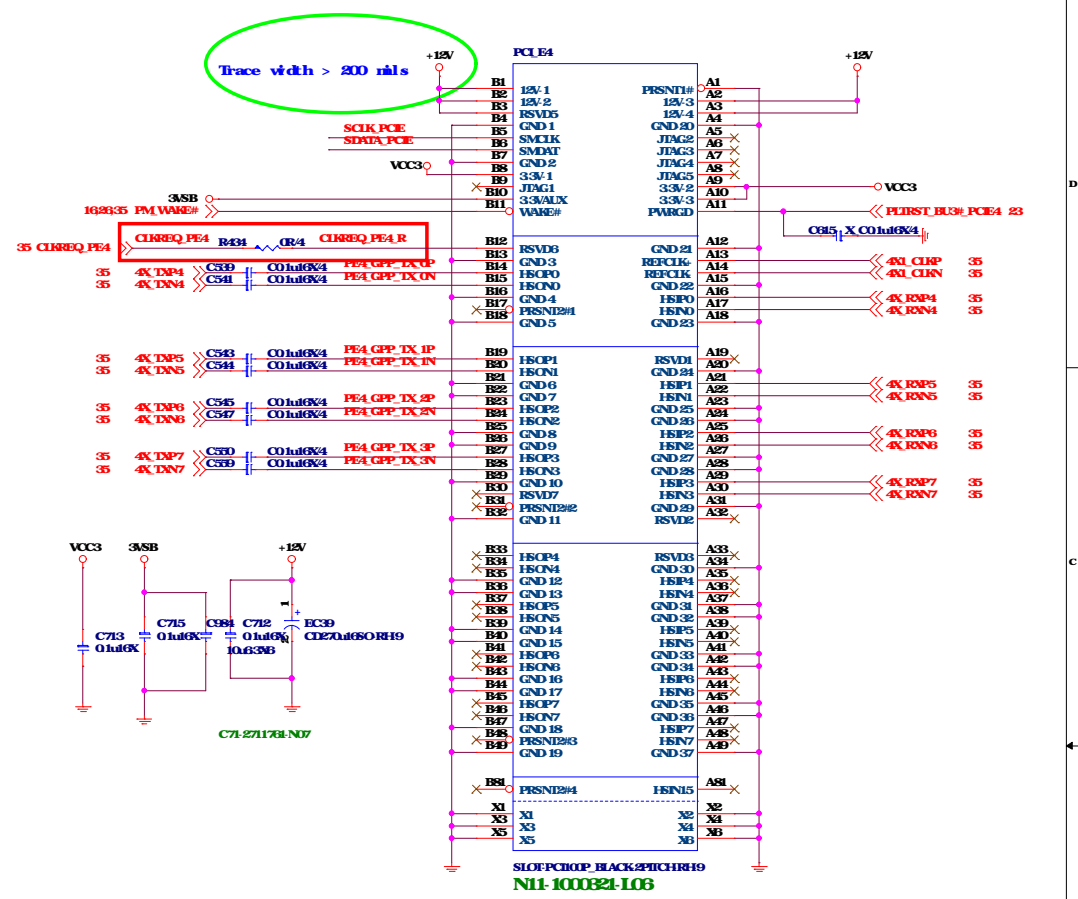


SMB SEL
GHO Default High

PCIEX1 12V 0.5A
3.3V weak 375mA

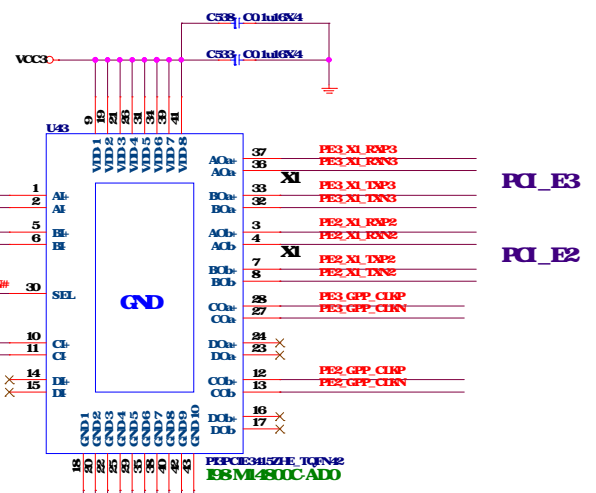


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PCI Lanes SW

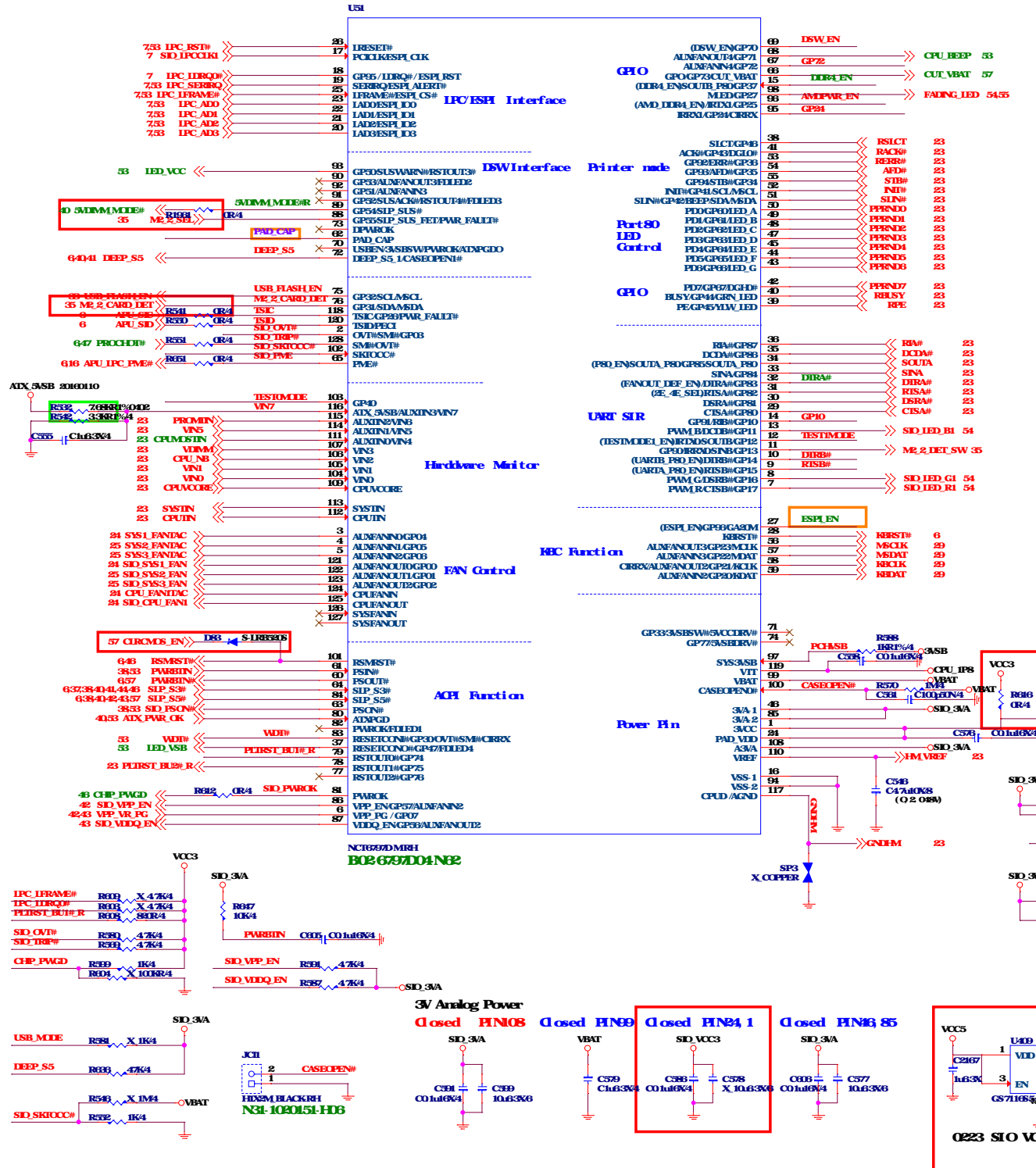
default (H): (PCI2)
Low (Ob/-) => (PCI3)
High (Ob/+) => (PCI2)



PCI Lanes control circuit

Manual LOW/Control PCI2
High : Control PCI3(def)
635 HW_BIOS_MODE
Select Auto or Manual mode
HWmode (stuff card)

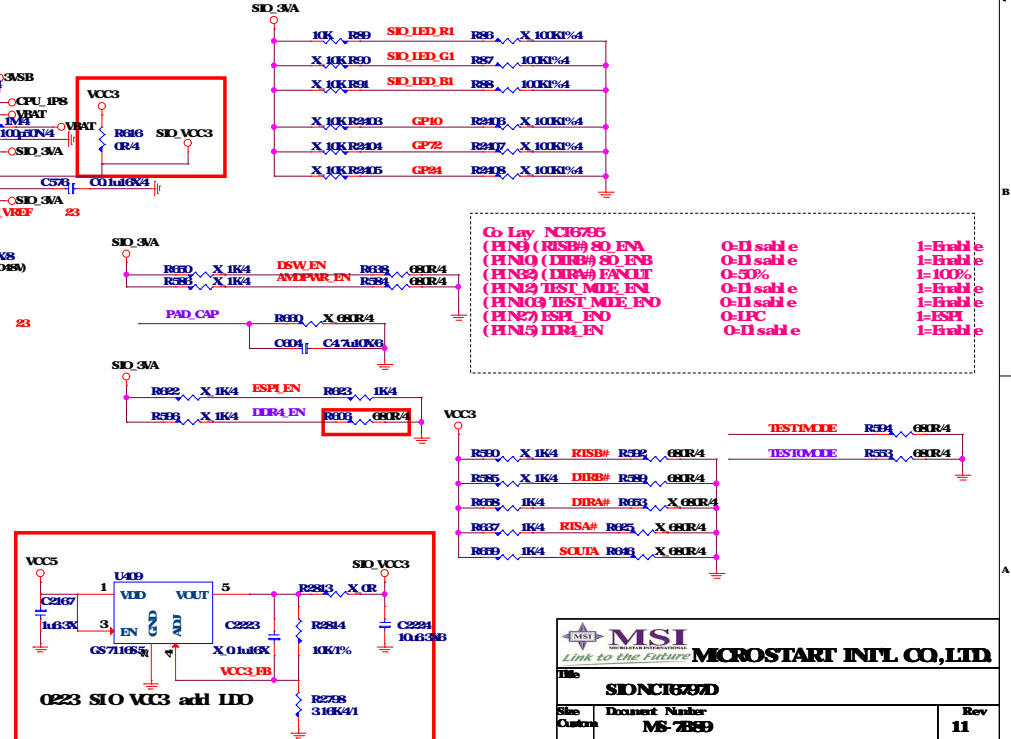
PCI Express x4 Slot *1	
+12V	- 21A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (nowake)	- 20mA
PCI Express x1 Slot *2	
+12V	- 1A
+VCC3	- 6A
+3V3_S5 (wake)	- 750mA
+3V3_S5 (nowake)	- 40mA



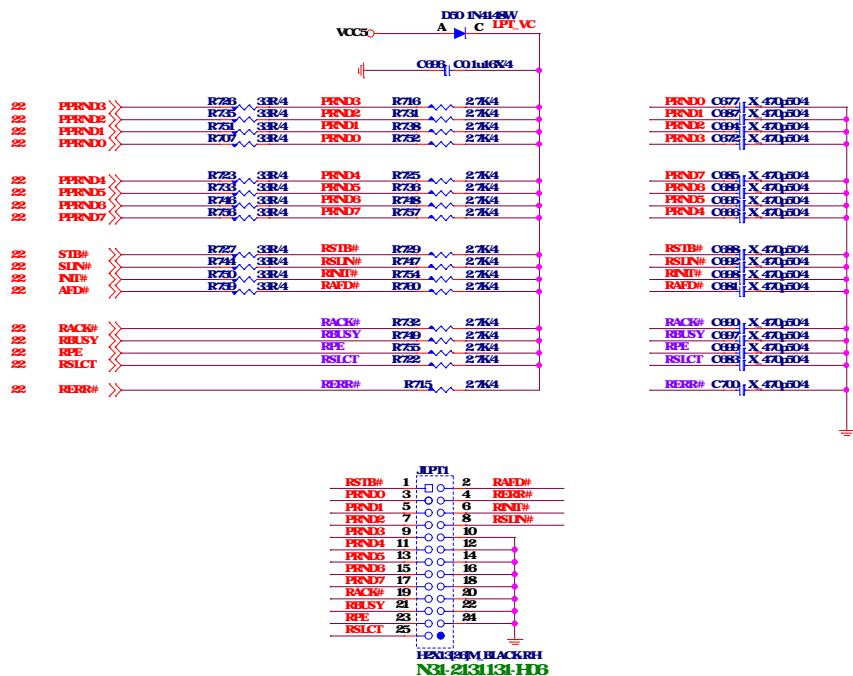
POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RISB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DIRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE_EN	TESTMODE	DISABLE TESTMODE	ENABLE TESTMODE	LRESET
15	6793 test point 6795 IDRA_EN	6793 test point 6795 IDRA_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 IDRA_EN 6795 ESLEN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RISA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMODE_EN 6795 FANOUT_DEF_EN	DIRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWRCK
34	P80_EN	SCUTA	ENABLE Non PORB80	ENABLE PORB80	LRESET
69	DSW_EN	DSWEN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMST
96	AMPVW_EN	AMPVW_EN	DISABLE AND PWR SEQ	ENABLE AND PWR SEQ	INTERNAL RSMST
103	TESTMODE_EN	VDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMST

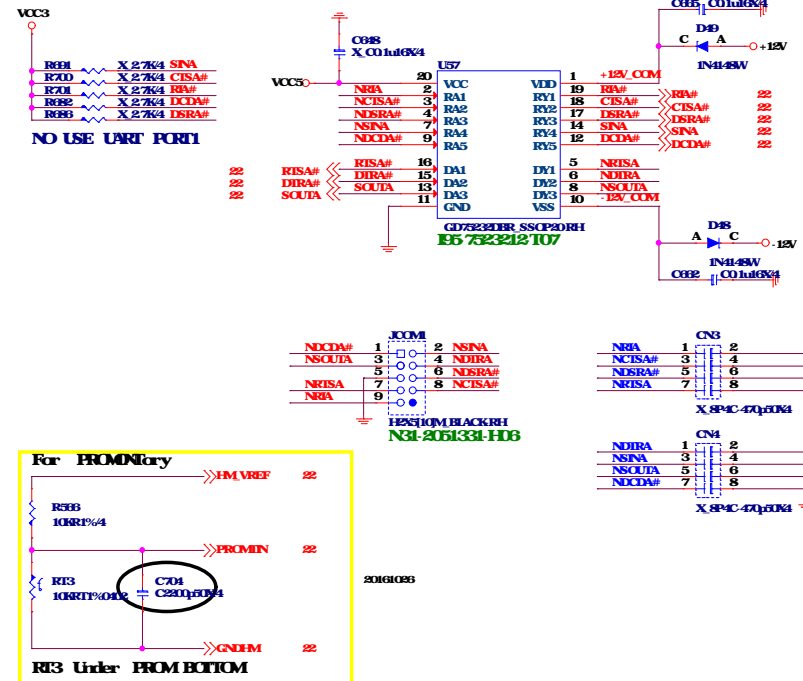
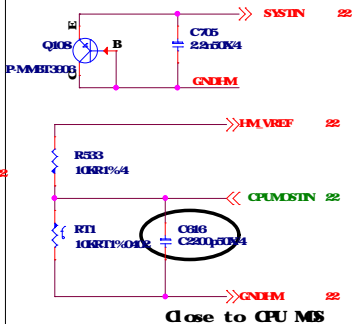
Note: If PIN34 strapping low/HIGH must programming IPT or GPIO



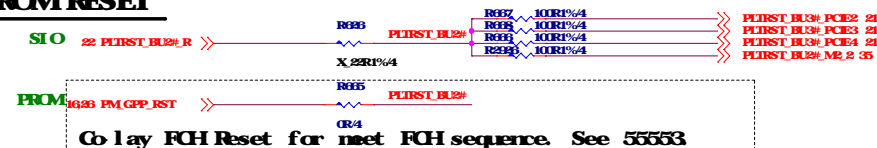
SIO HM Voltage over 2.048V will not detect



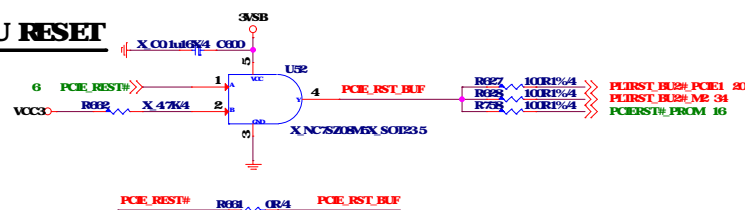
COM PORT



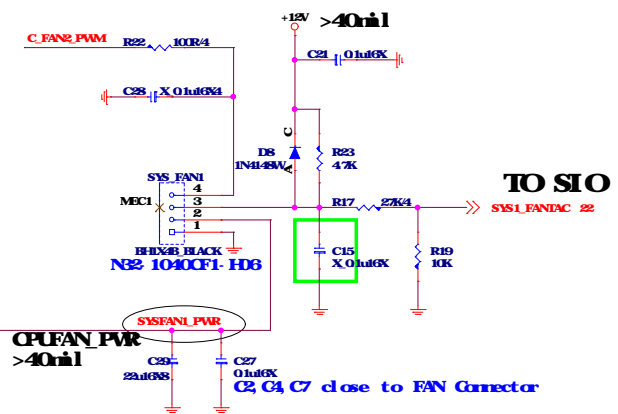
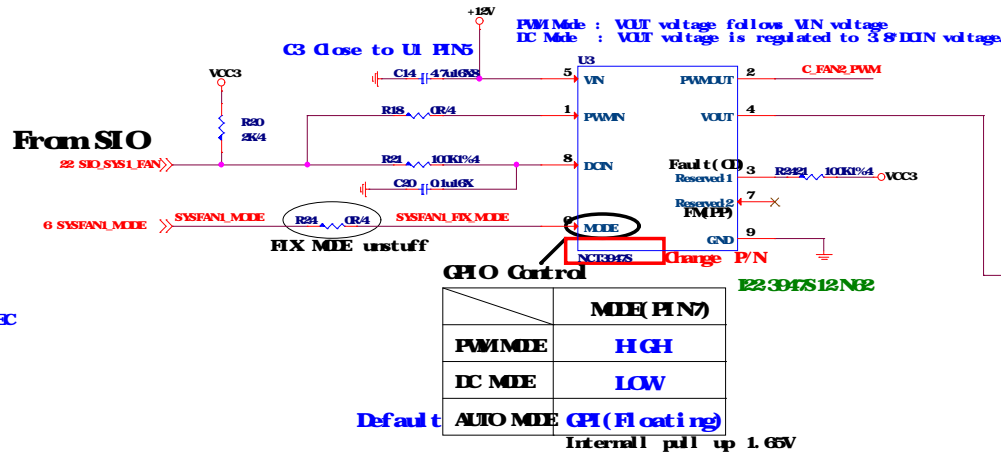
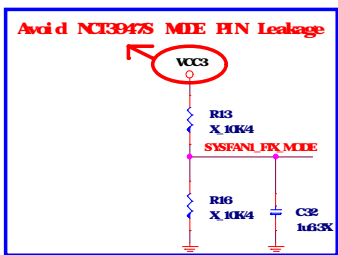
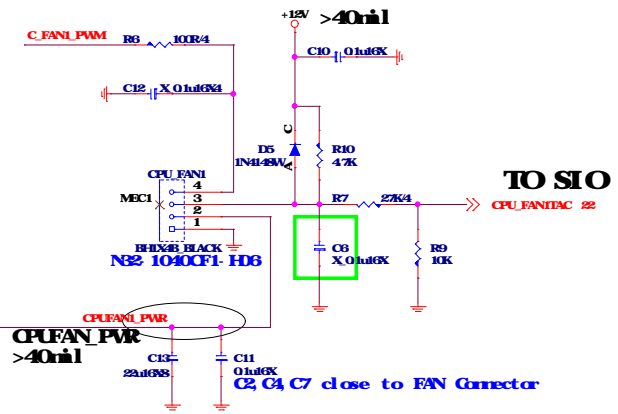
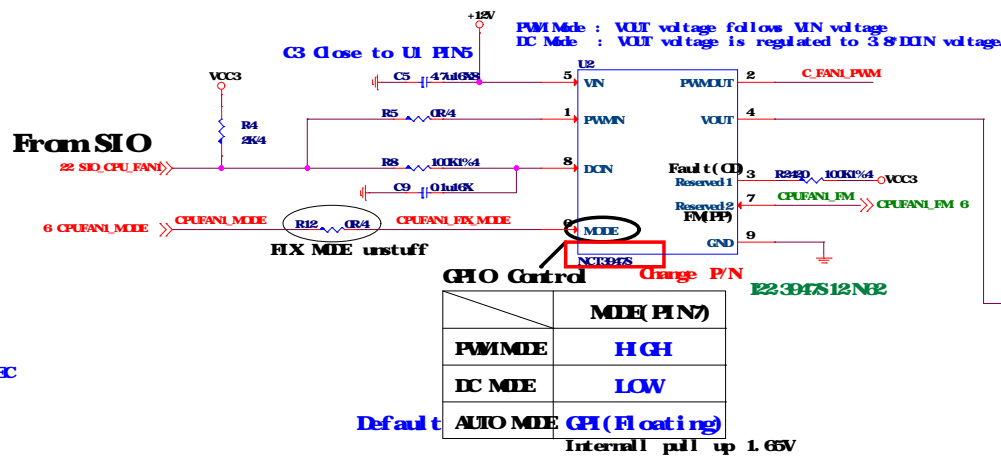
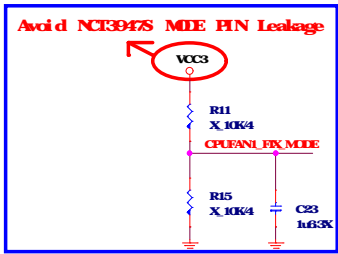
FROM RESET



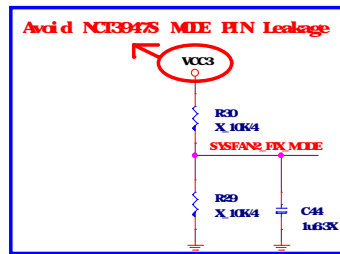
CPU RESET



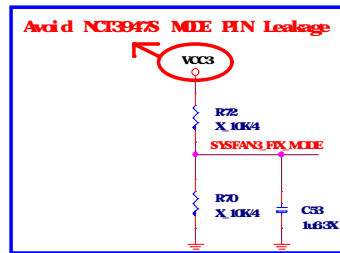
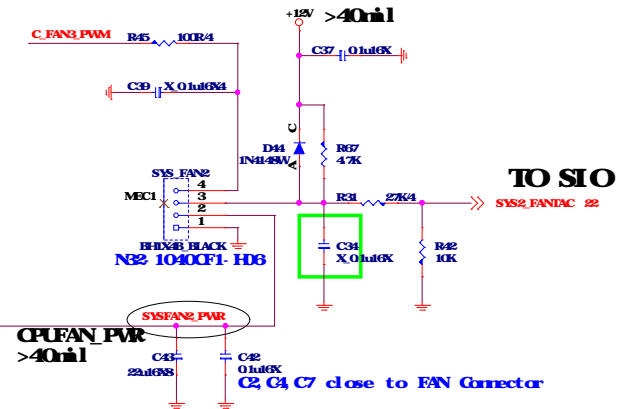
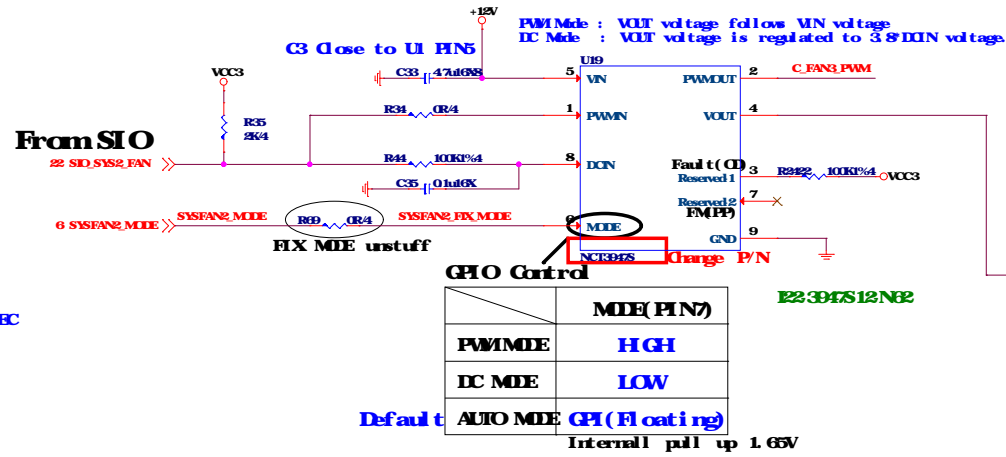
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MDE
2 GPIO BD PW MDC MODE



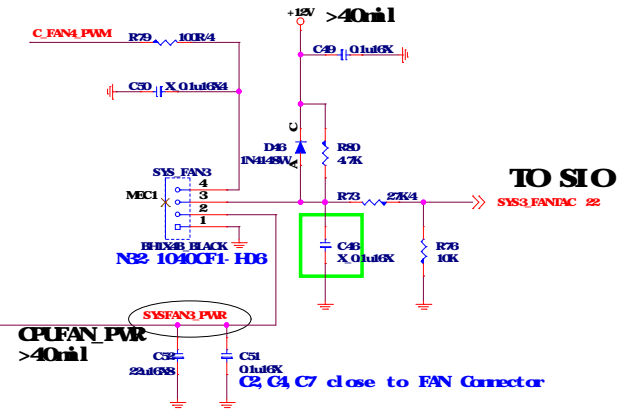
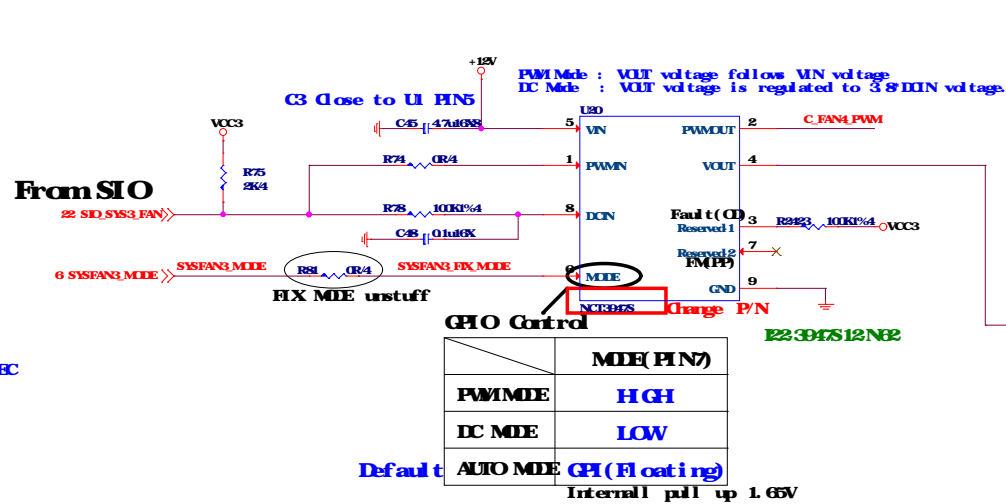
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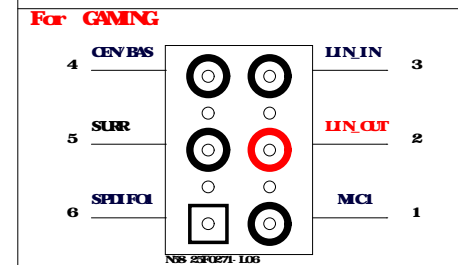
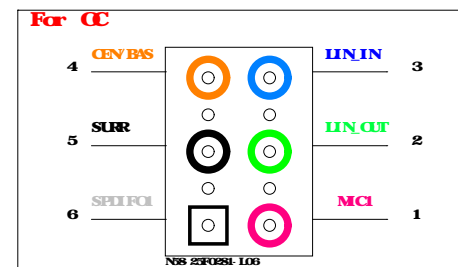
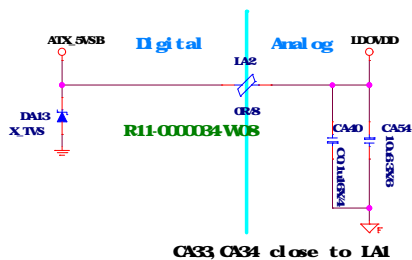
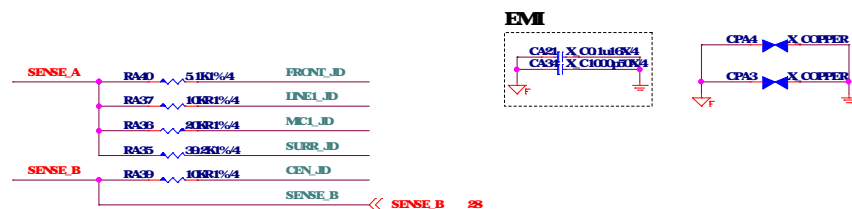
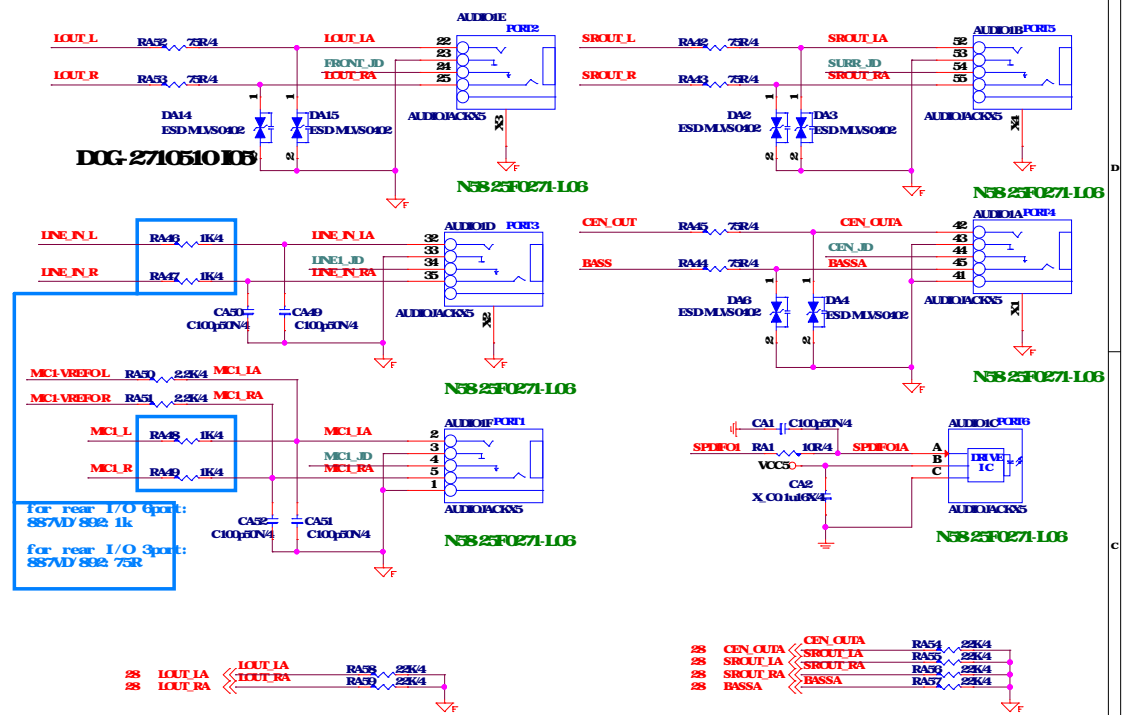
Reserve For FLXTC or PWMDE USE By FMSPEC



Reserve For FLXTC or PWMDE USE By FMSPEC

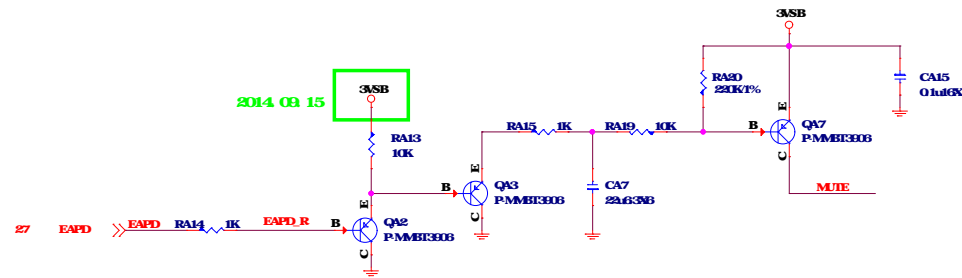


Follow APU power well



Rear Line OUT De-POP circuit

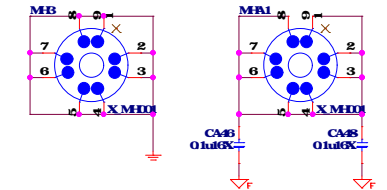
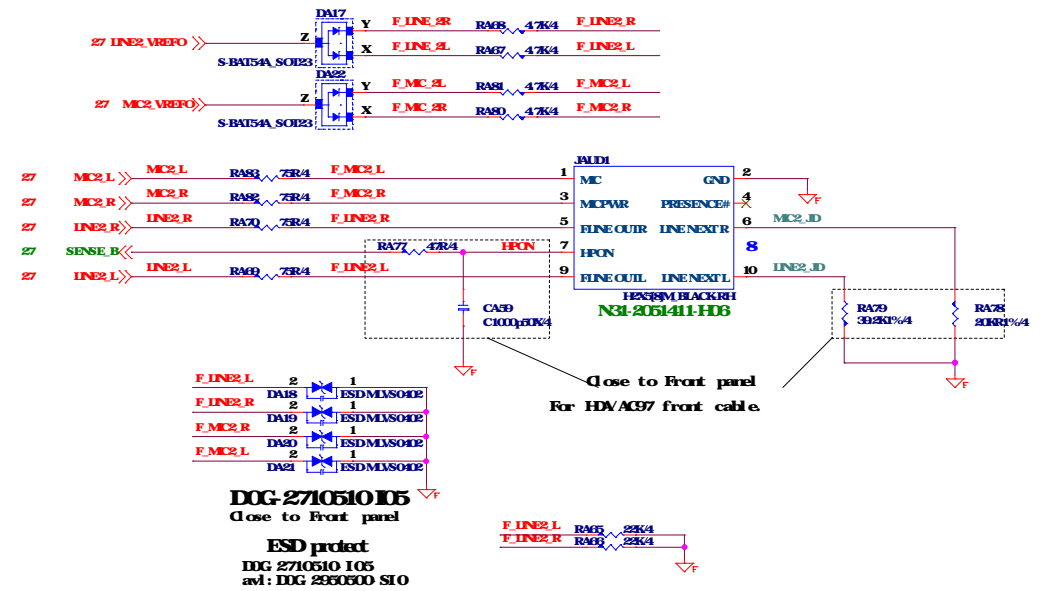
De-pop circuit for Rear Line out & Front Headphone out)



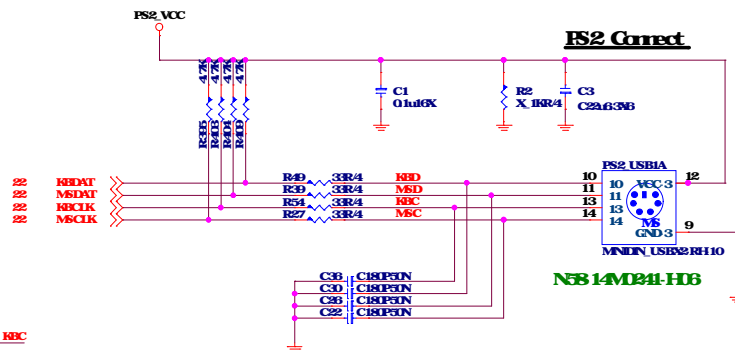
Digital



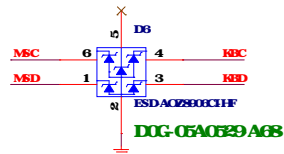
(add de-pop circuit by PMspec or customer request,
NOTE add de-pop circuit need to change CA5, CA6, CA7, CA9 to TVS)



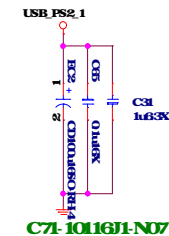
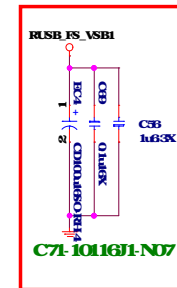
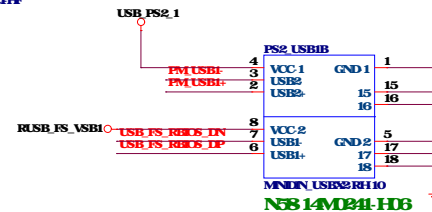
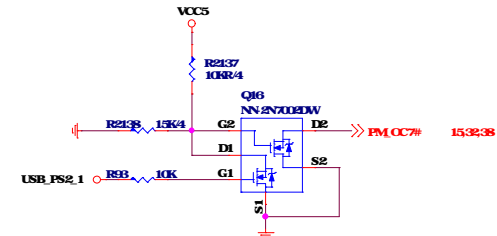
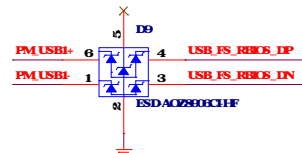
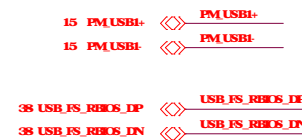
FS2+USB



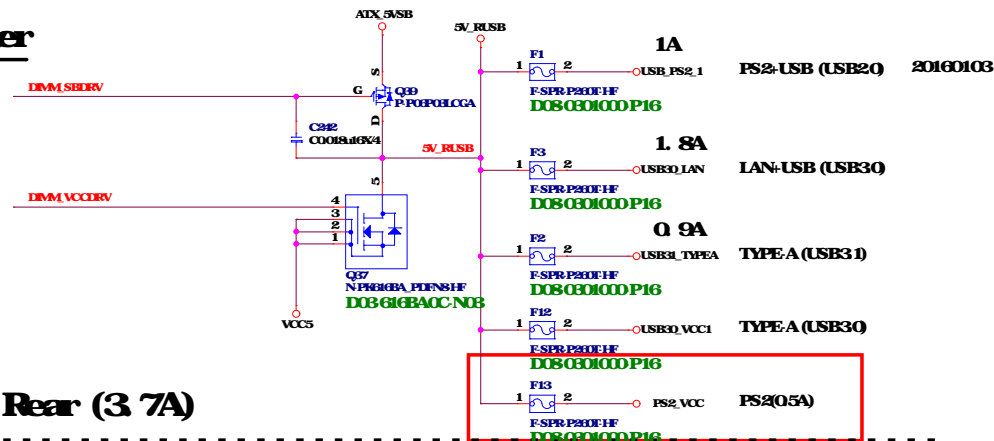
TVS P/N
DDG-45B0510-114



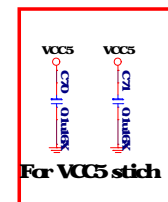
Layout note:
Q21 must close to TVS pin5
TVS must near RB1M1 connector and route without branch
Varistor must close to TVS and route without branch



USB Power



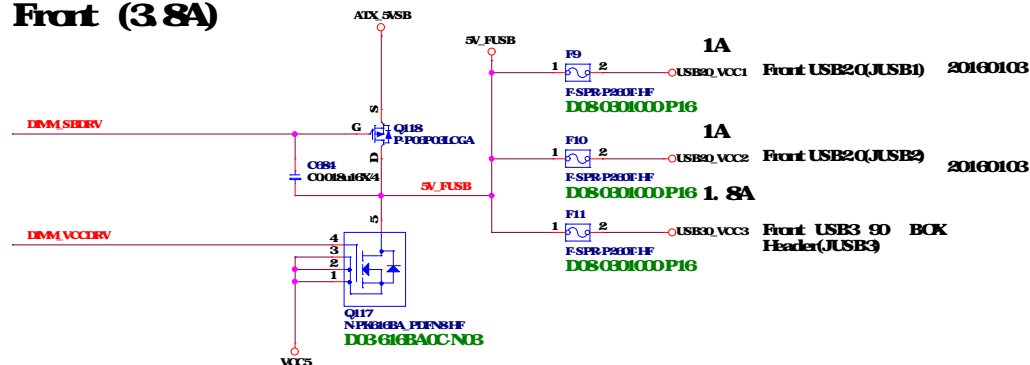
40 DIMM/VCC1RV << DIMM/VCC1RV
38-40 DIMM/SB1RV << DIMM/SB1RV



For VCC5 stick

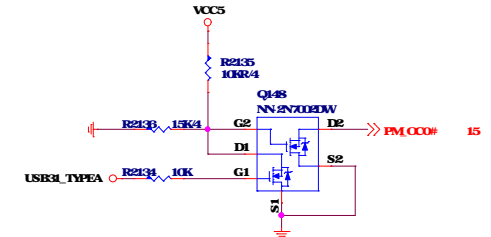
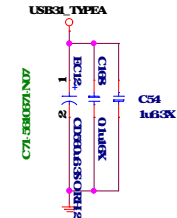
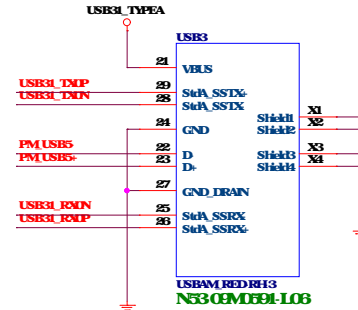
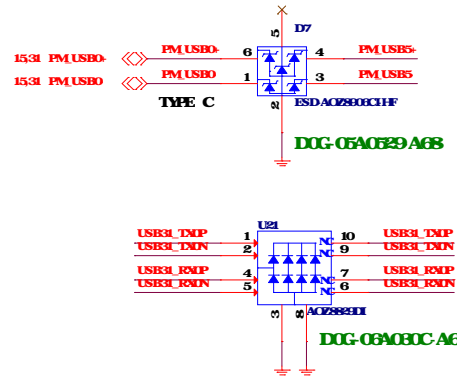
Rear (3 7A)

Front (3 8A)

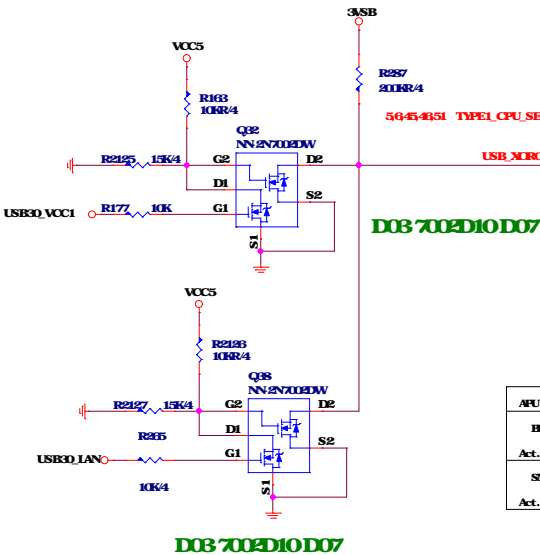


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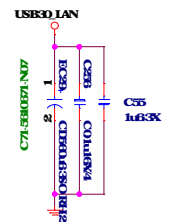
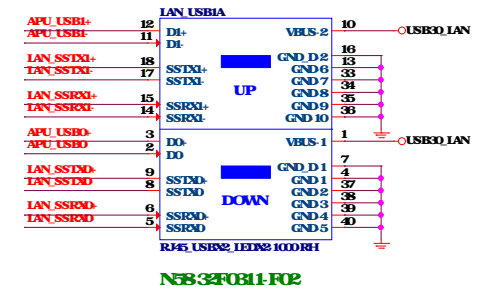
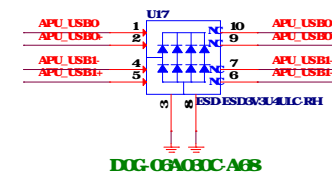
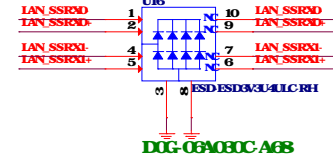
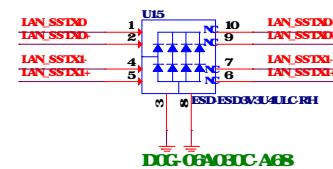
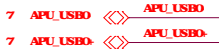
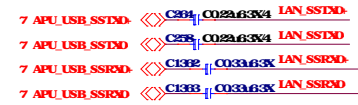
TYPE A USB 3 1



LAN+USB (USB3 0)



APU TYPE	CORETYPE	1	USB_OC0	APU_USB_OC#0
BR	0	0	0	0
Act. Low	0	1	1	1
SMBV	1	0	1	1
Act. High	1	1	1	0

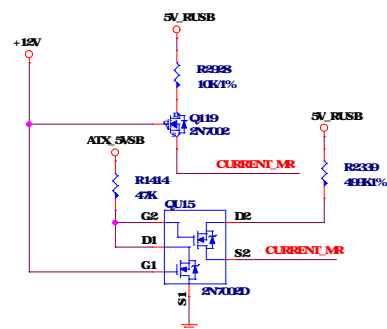


USB 3.1- Type C

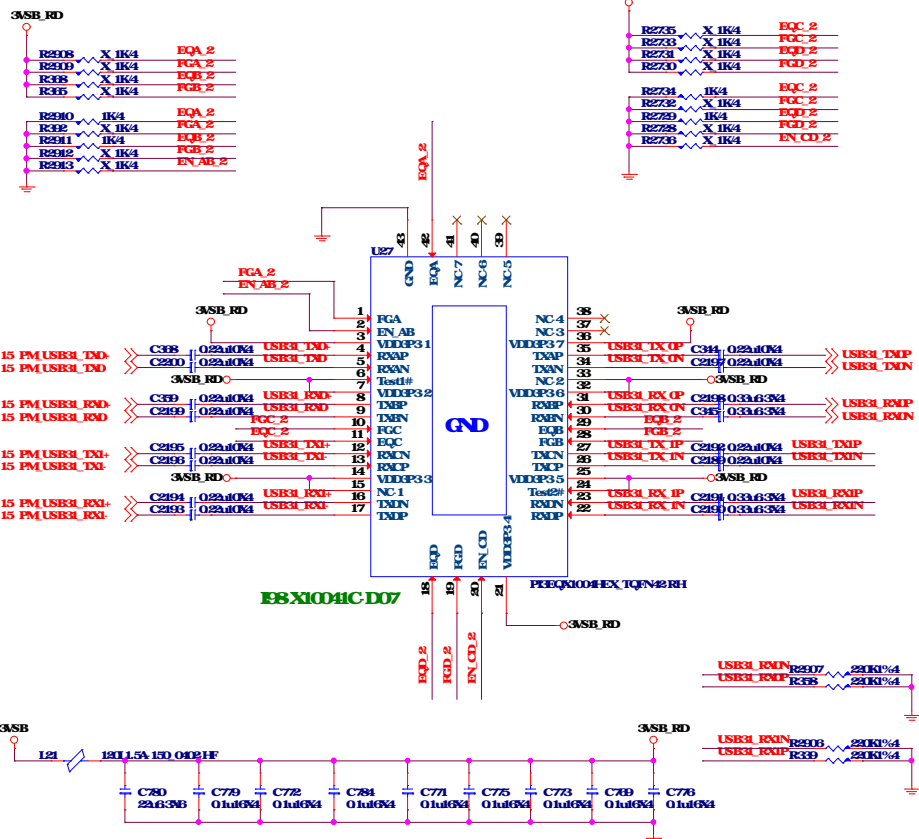
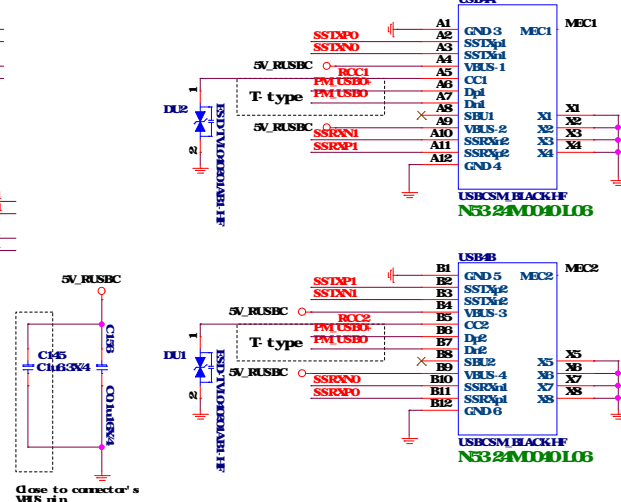
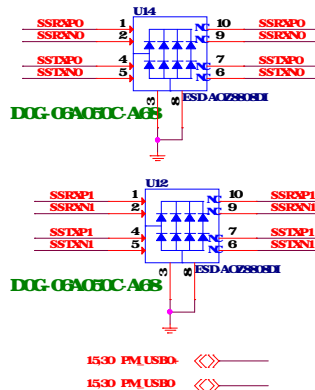
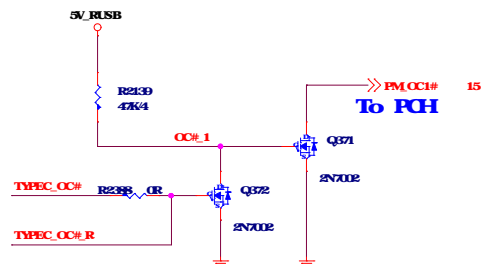
5V@3A

Current Mode

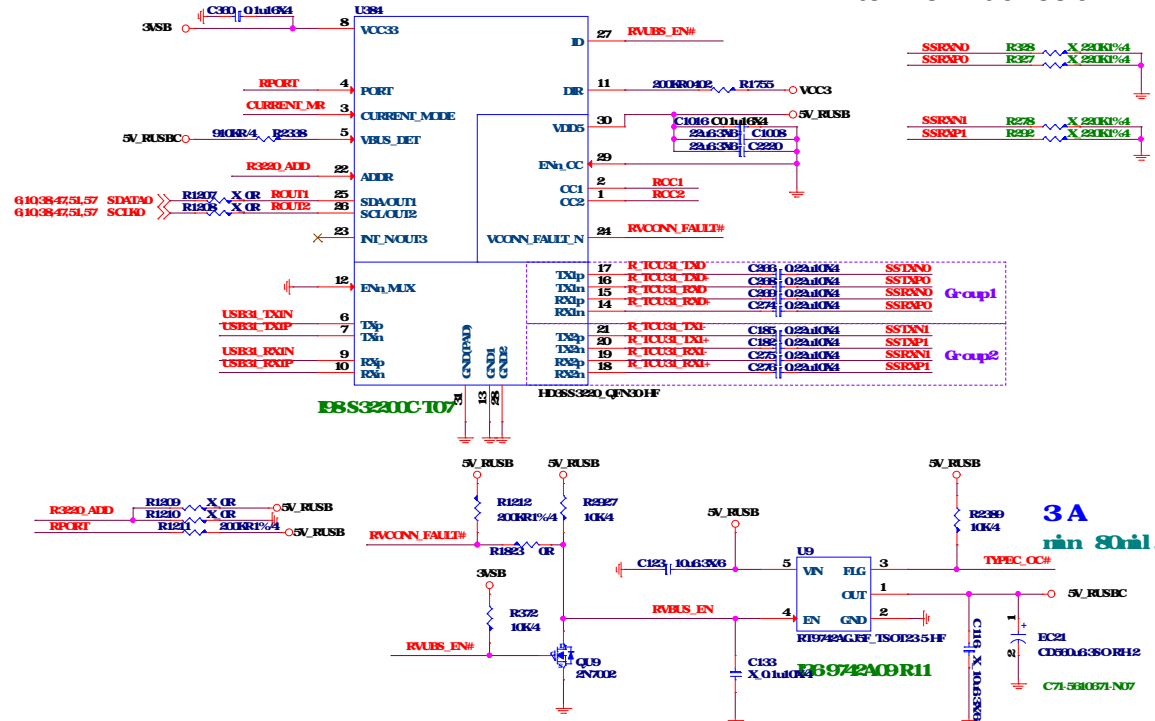
L - Default for 900mA
M - Mid (500K) for 1.5A
H - High (10K) for 3A

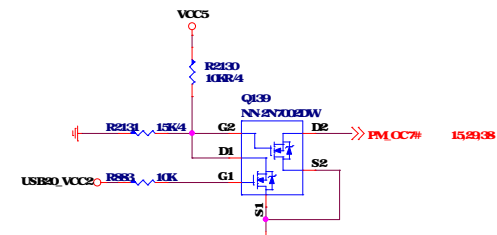
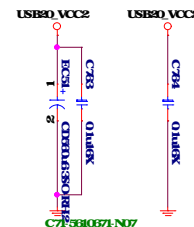
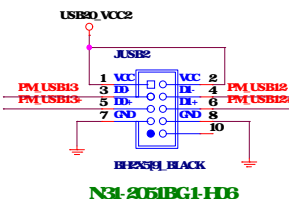
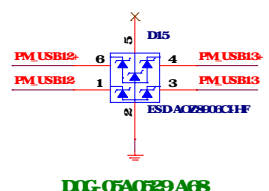
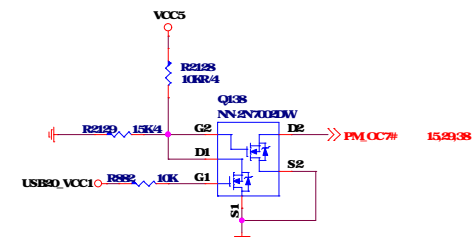
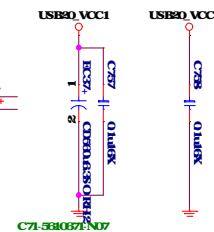
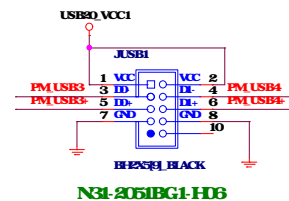
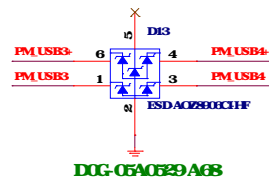
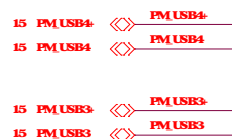
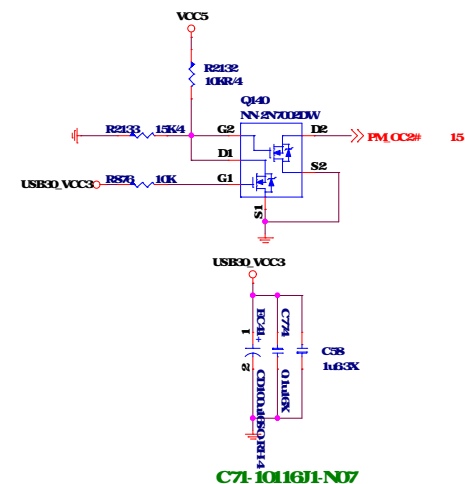
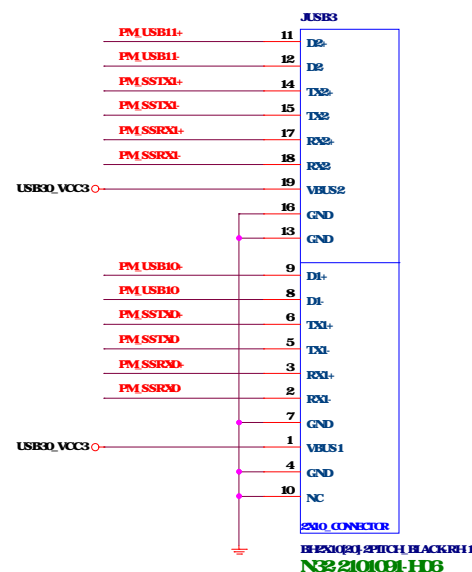
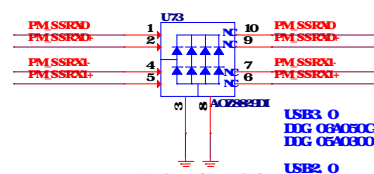
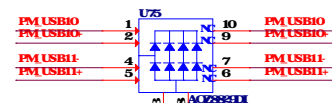
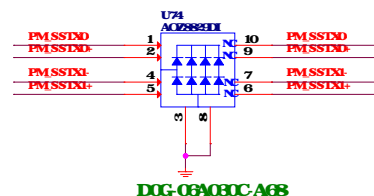
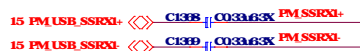
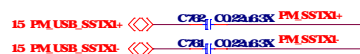
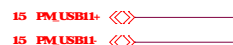
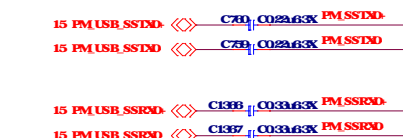


VBUS CC#

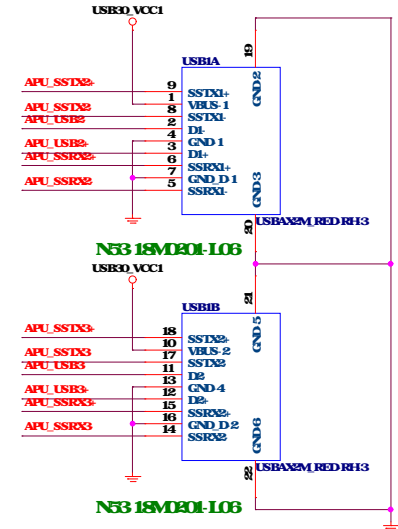
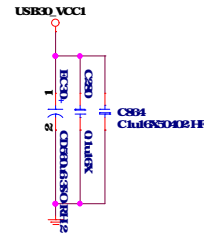
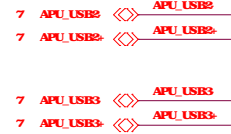
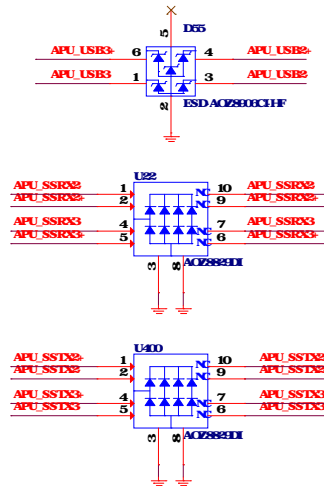
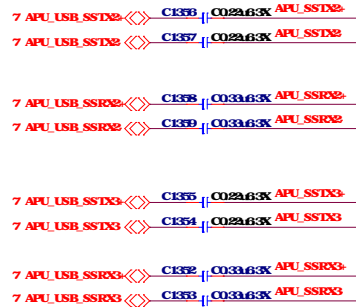


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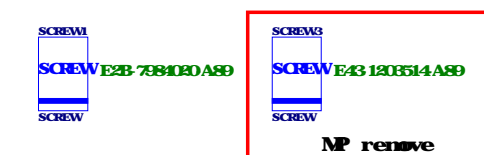
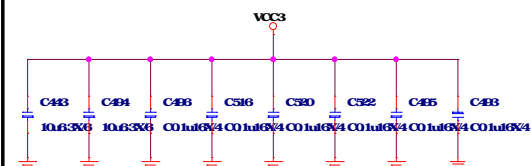
Front USB20**Front USB3 1 GEN1**

USB 0



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3 3V@2 5A

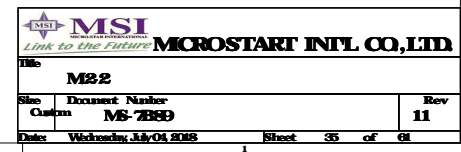
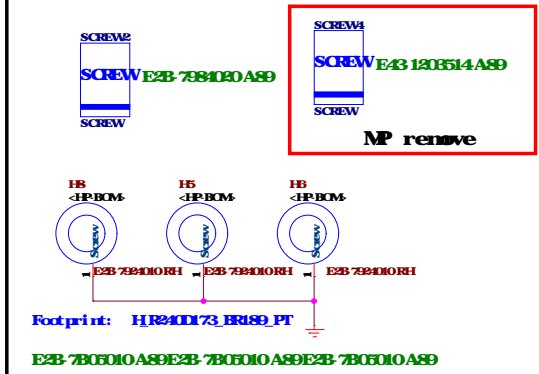
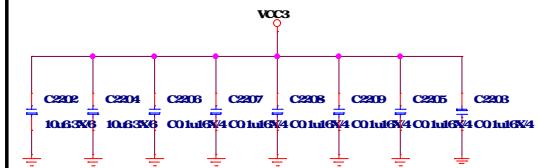


Footprint: H_R240D173_BR189_PT

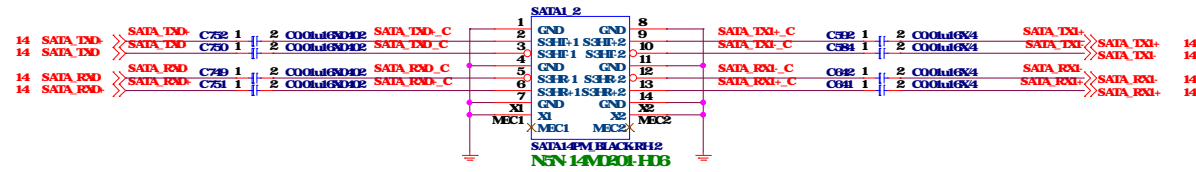
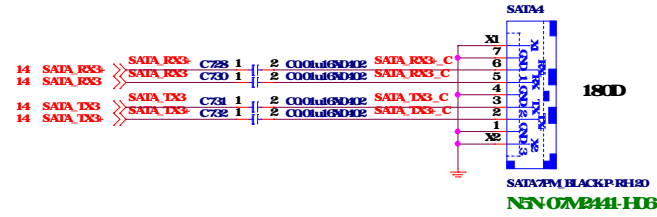
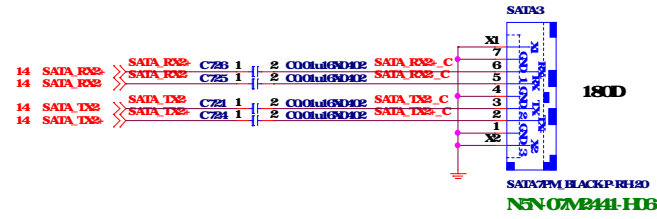
E2B-7B05010A89E2B-7B05010A89E2B-7B05010A89

SW
HM2 POIE
L: M2 SATA

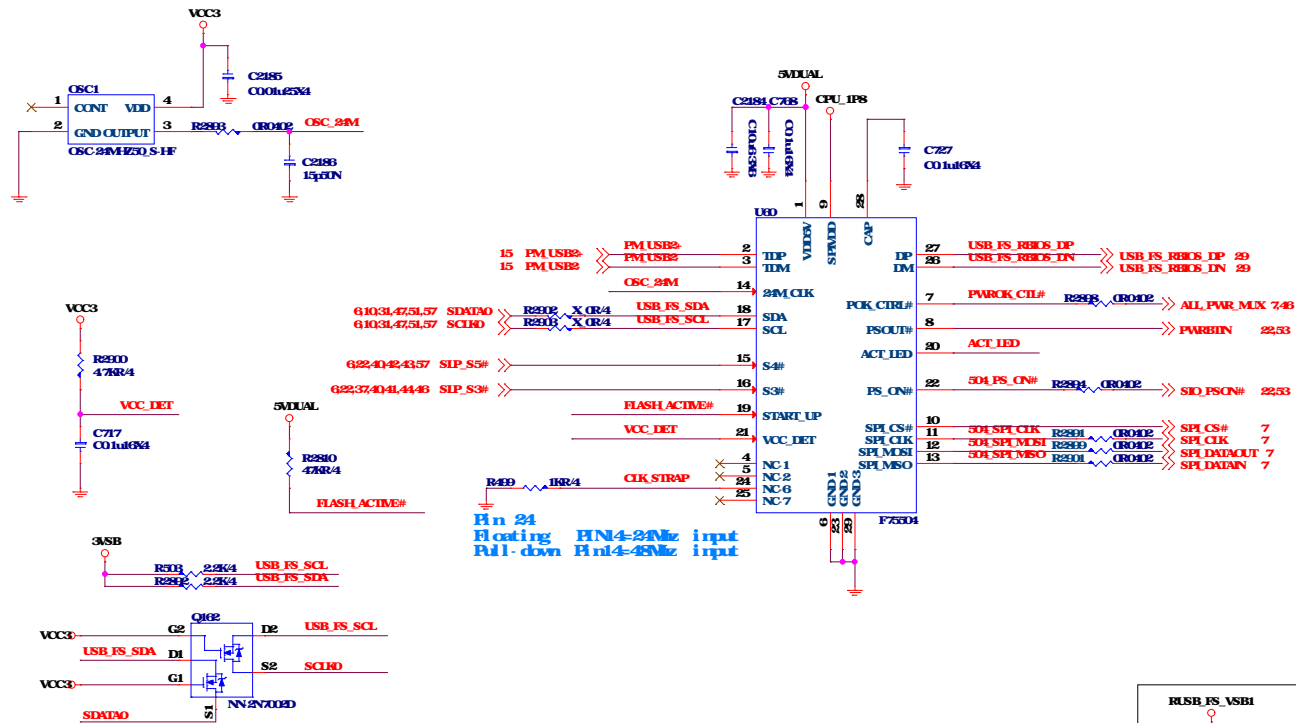
3 3V@2 5A



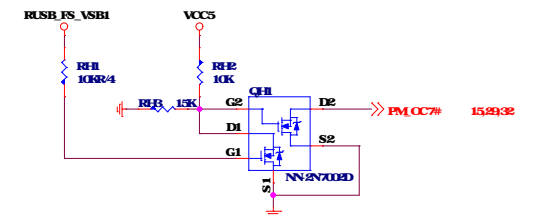
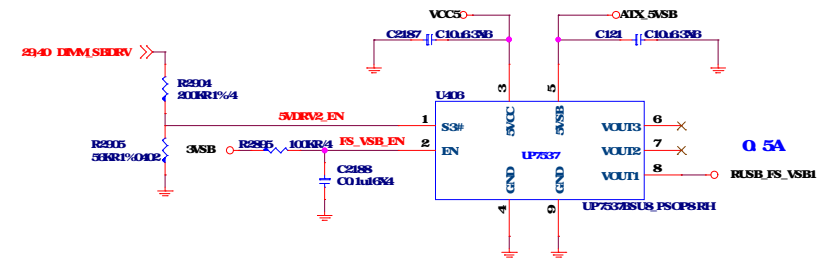
SATA Connector



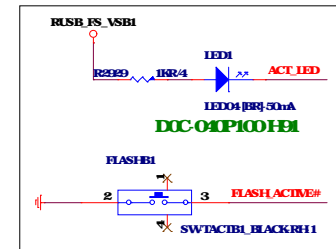
USB Flash BIOS

Hbst USB connector

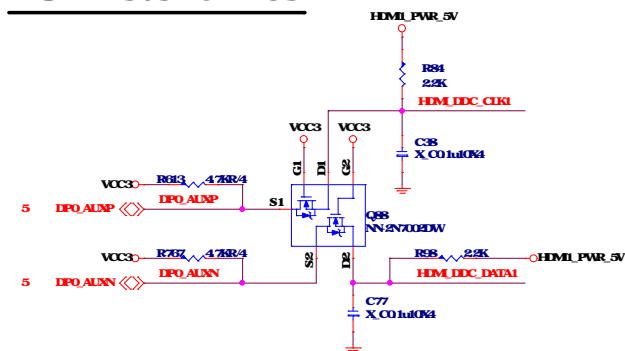
REAR Flash BIOS USB



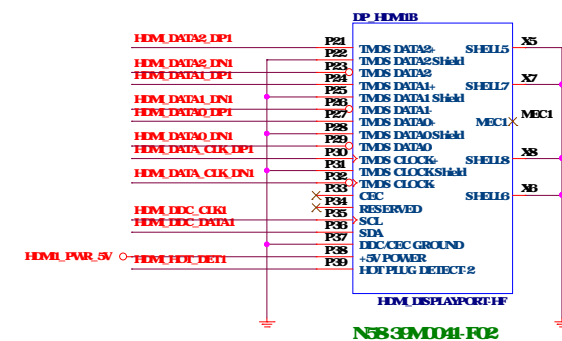
OC# signal correct to
SB OC pin



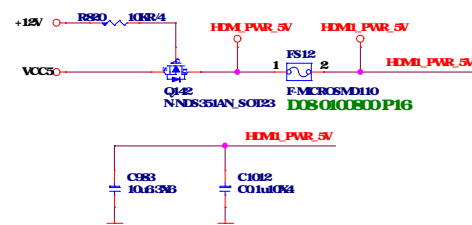
REF2
PCB
XSP4R-1K0608

For HDM 1.4

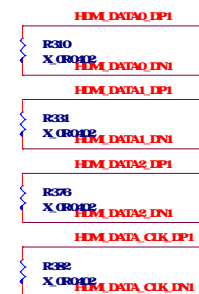
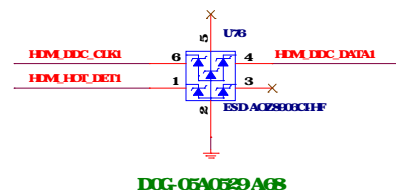
Connector

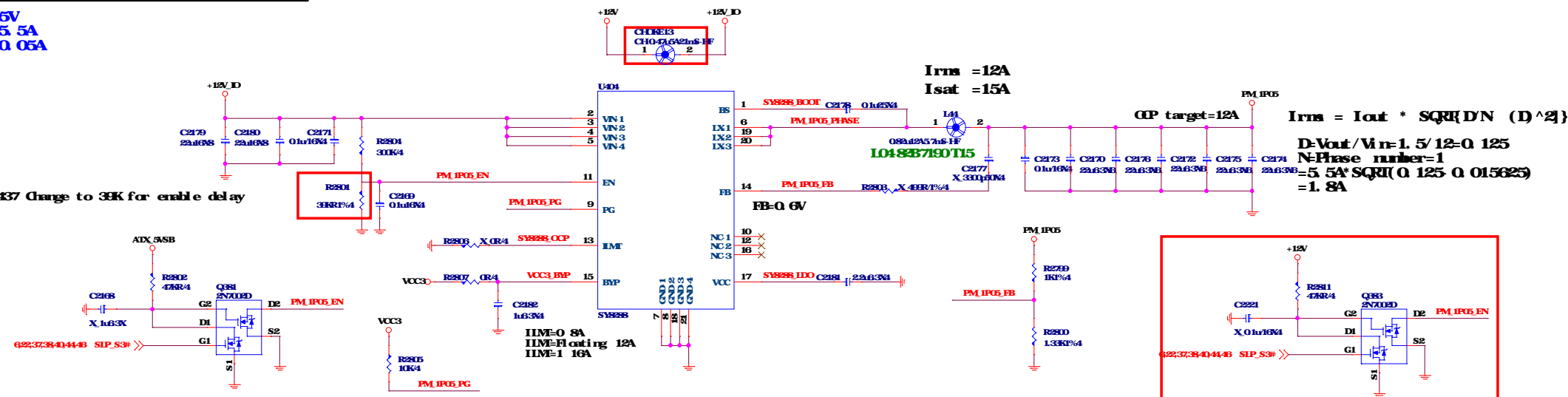


HPD Circuit

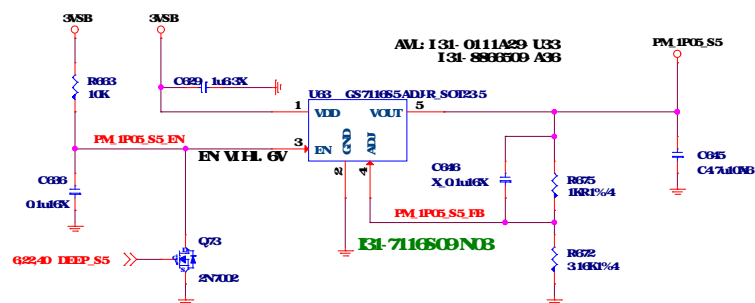


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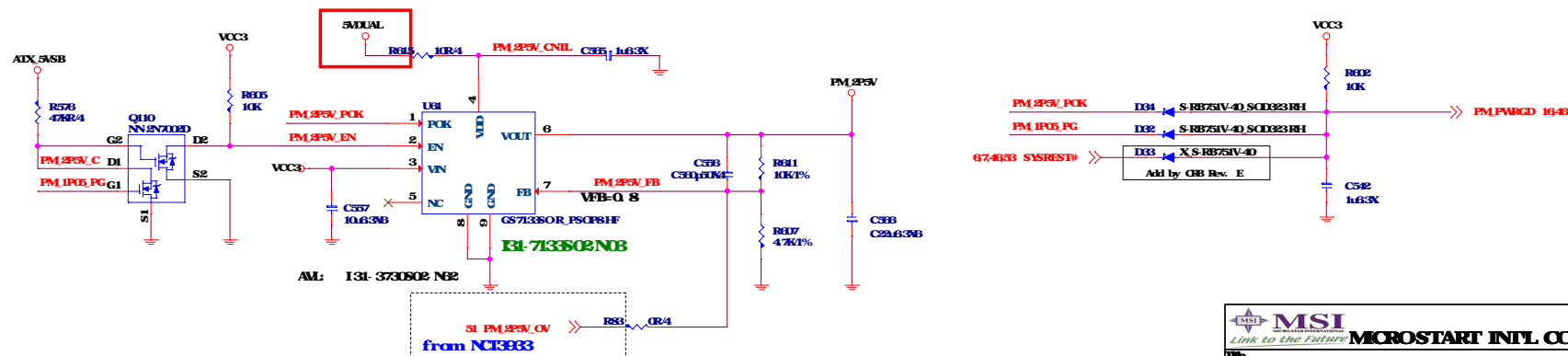
For EM

R437 Change to 39K for enable delay

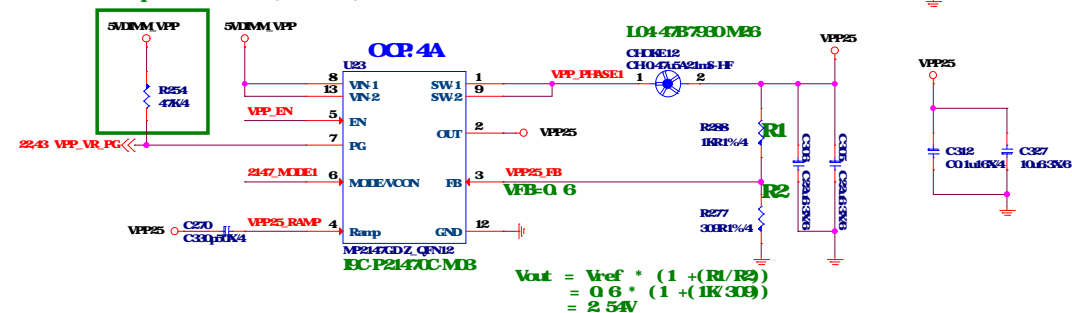
Q 05A



2.5V; 900nA

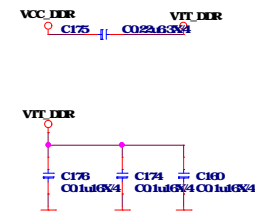
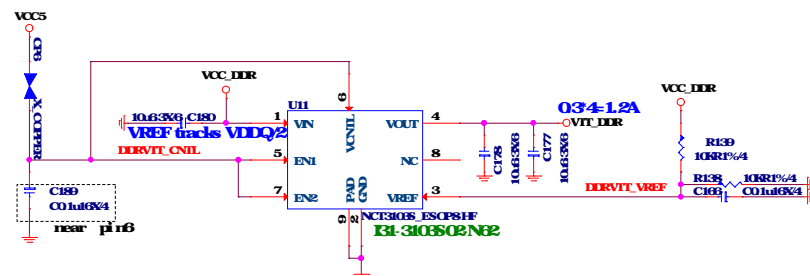


2 5V@2 24A



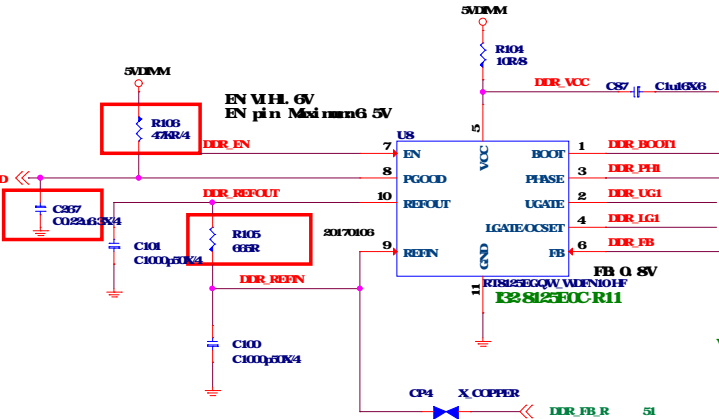
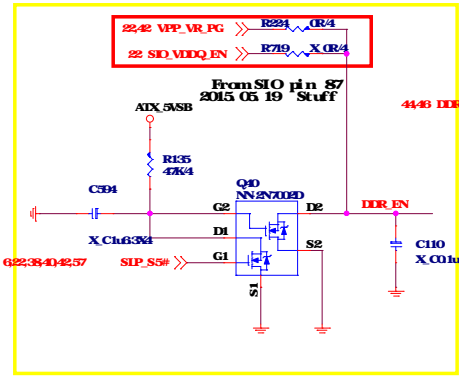
DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

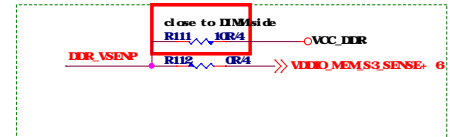


DDR4_1.36V@26 2A

15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT



$$V_{out} = V_{ref} * (1 + (R1/R2))$$
$$= 0.8 * (1 + (4.12k/6.65k))$$
$$= 1.2089V$$



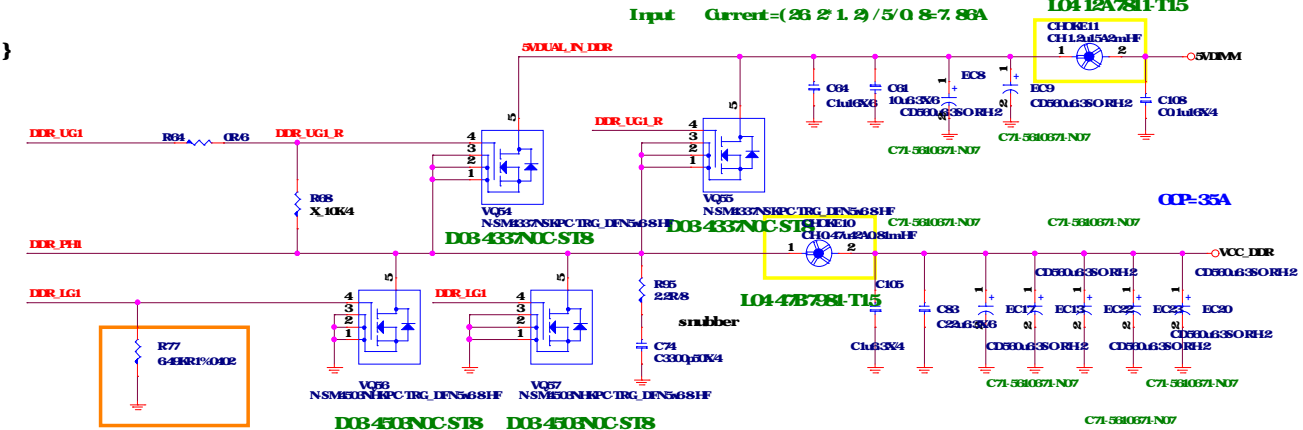
640-45-43 AFU_AMR1 >> D27 S-1B75IV-40 DDR_EN

EN VHL 6V
EN pin Mod mm6 5V, RECOMMENDED 3.6V

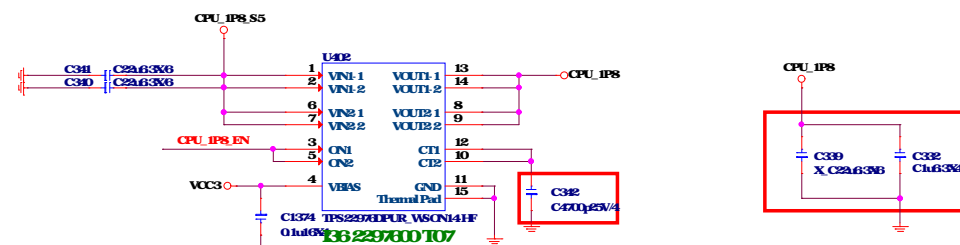
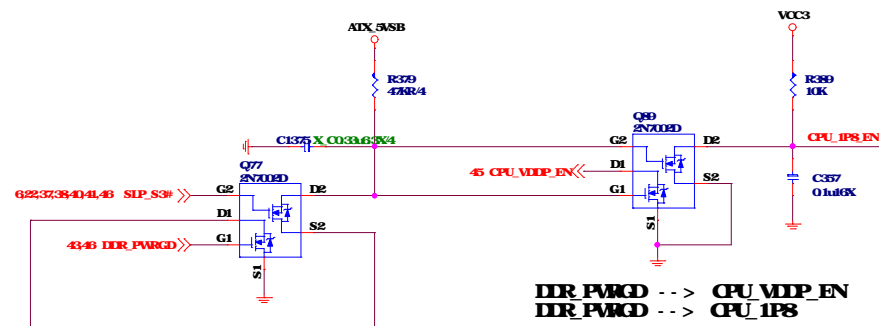
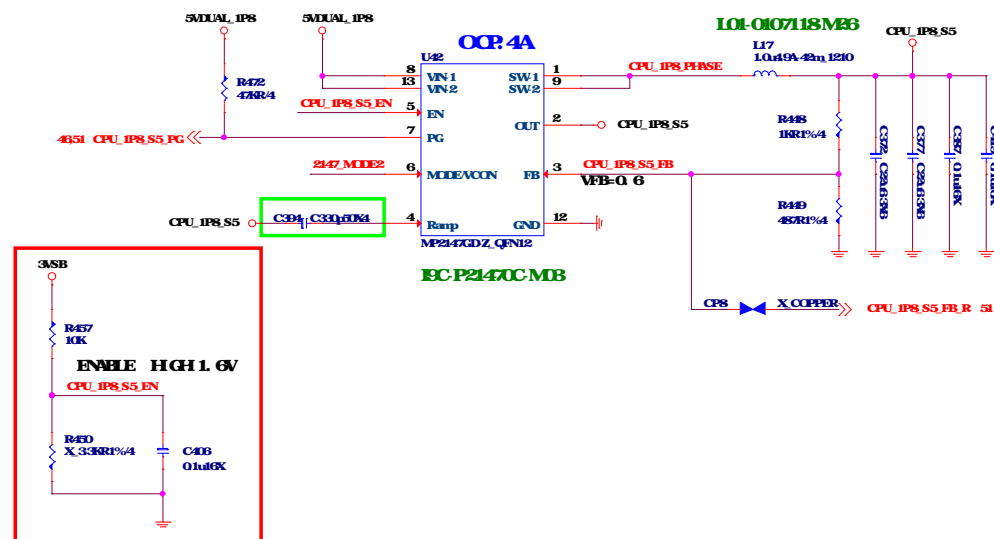
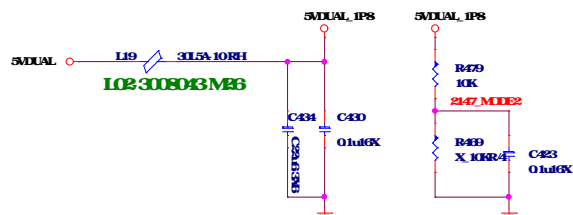


$$EDC I_{rms} = I_{out} / N \sqrt{N(1-N)}$$

CORE
D=Vout/Vi n=1.2/5=0.24
N=Phase number=1
=26.2/1*sqrt(0.24*[1-0.24])
=11.189A

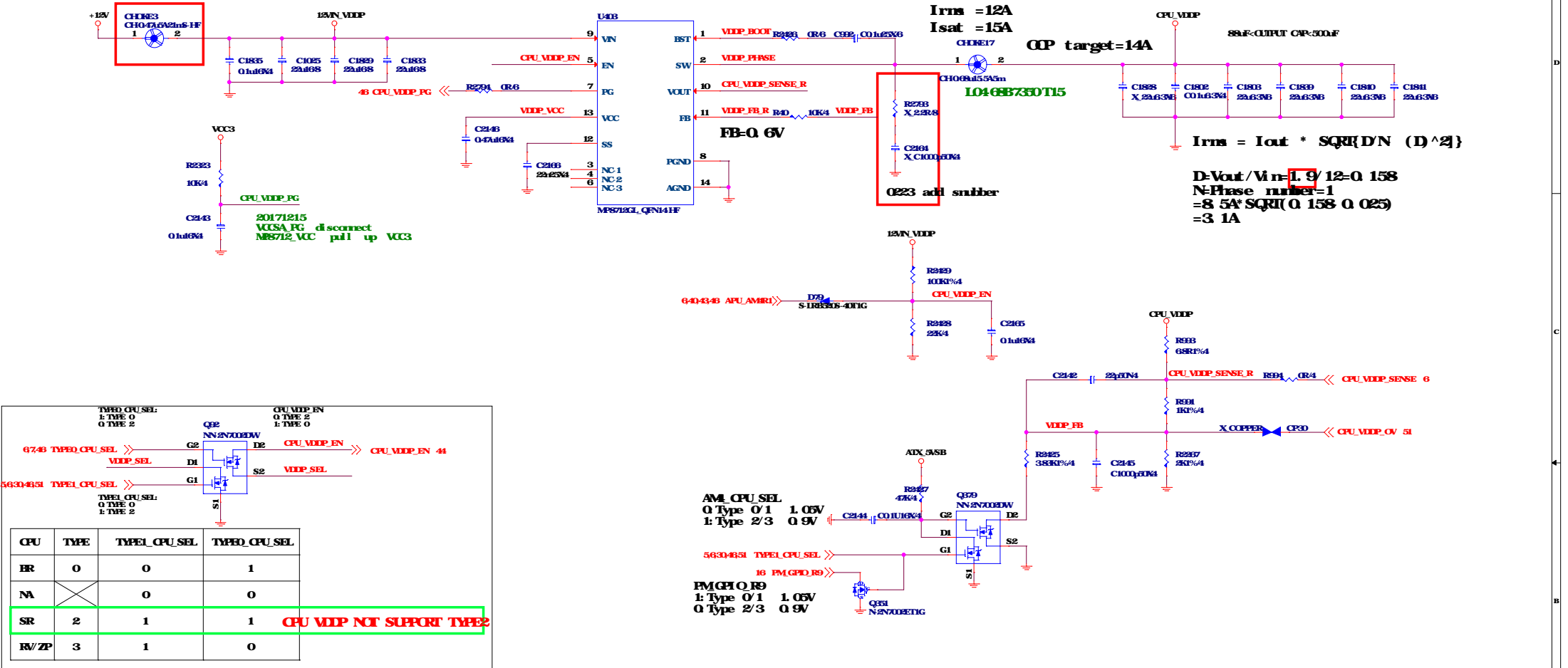


$$OCP = 26.2A * 1.5 = 39.3A$$
$$R_{DS(on)} = OCP * R_{DS(on)} / 10A$$
$$= 35A * 1.65m\Omega / 10A$$
$$= 5.77K$$

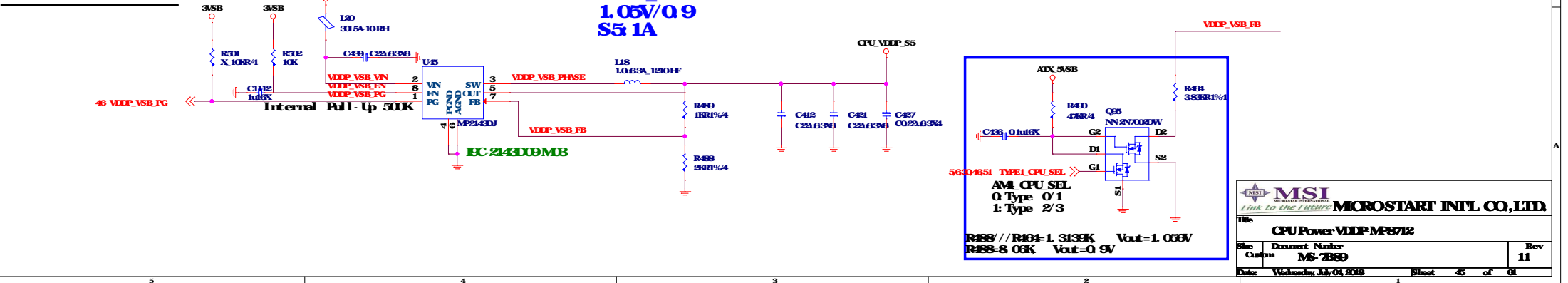
$$0.5A + 2.0A + 0.9A = 3.4A$$


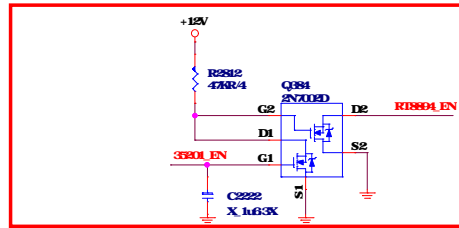
Adjustable Rise Time
 $SR = 0.42 / CT + 66$
 SR is the slew rate in (s/V)
 CT is constant value on CT pin (in pF)
 The units for the constant 66 is in
 (s/V)

CPU_VDDP_S0 1.05V/0.9 5A

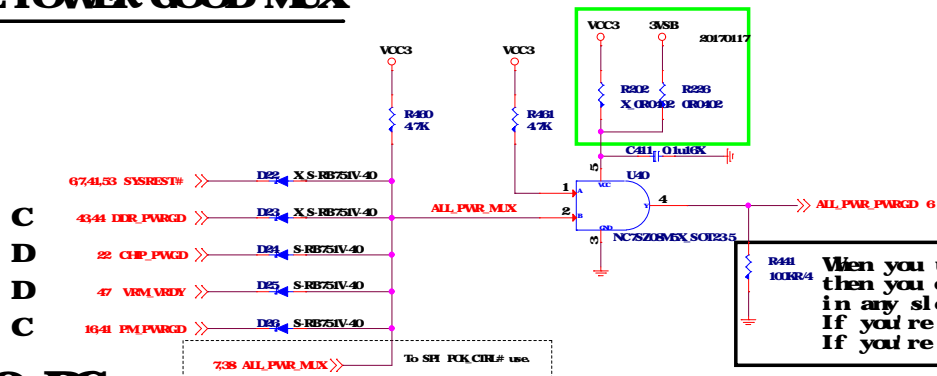


CPU_VDDP_S5

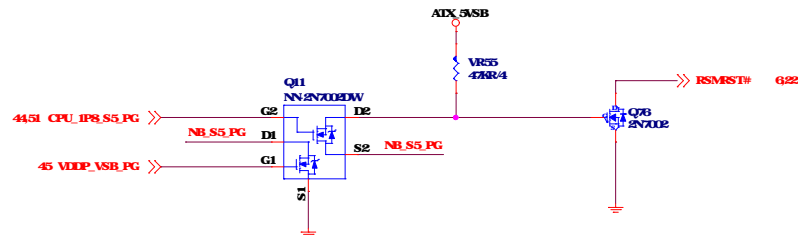




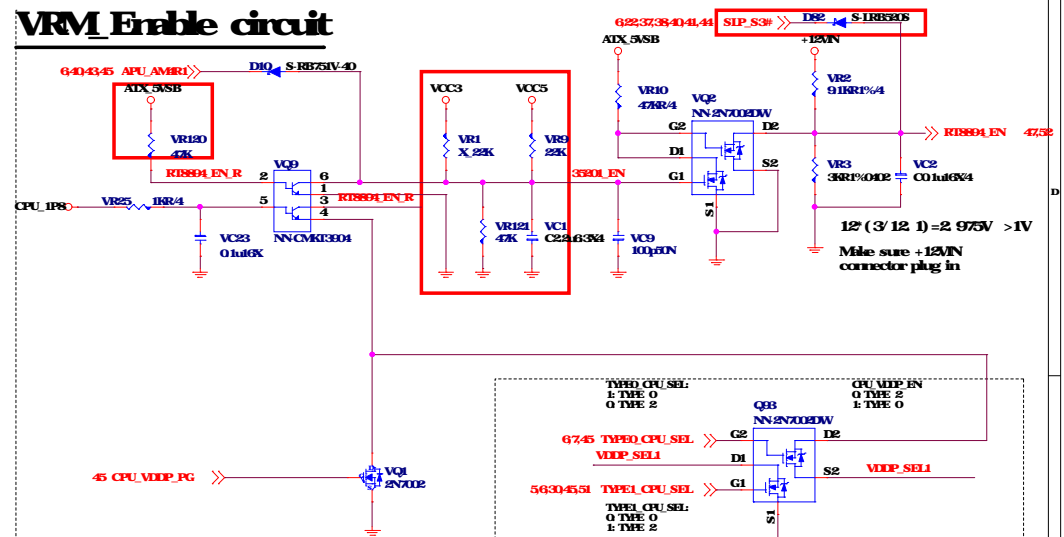
ALL POWER GOOD MUX



S0 PG
S5 PG



VRM Enable circuit

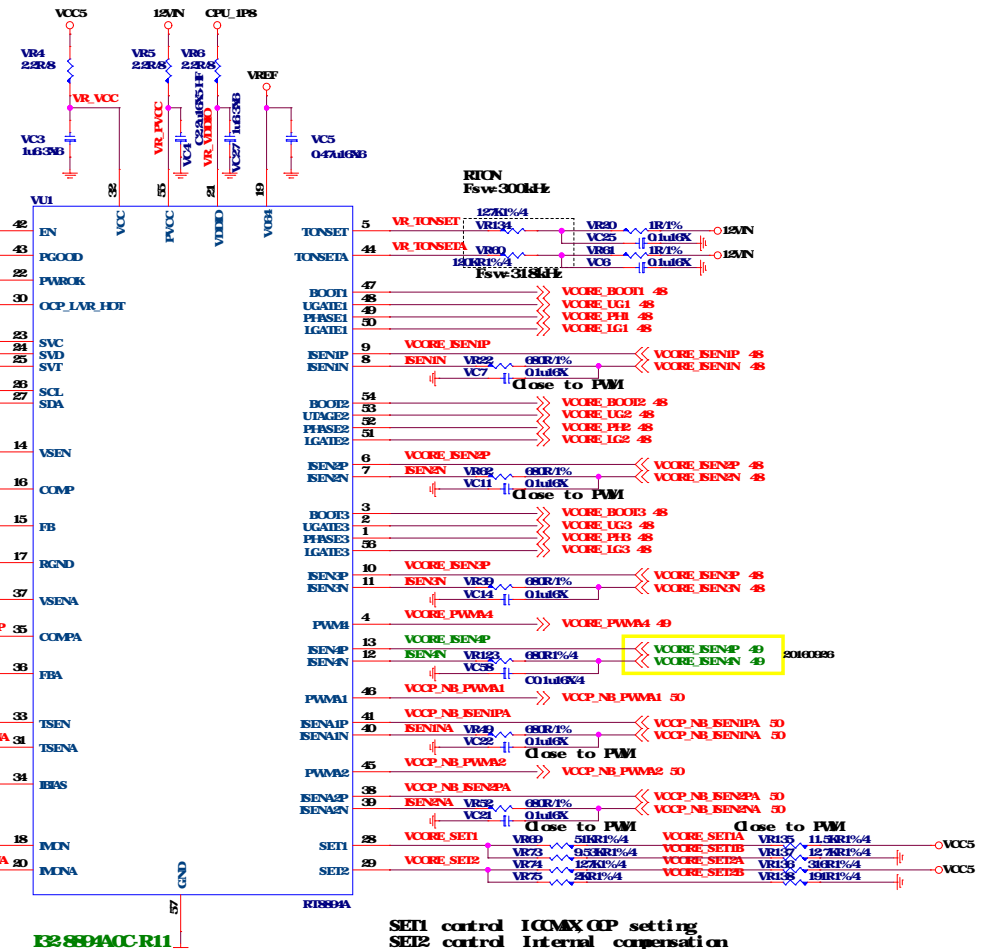
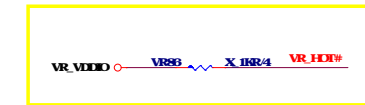
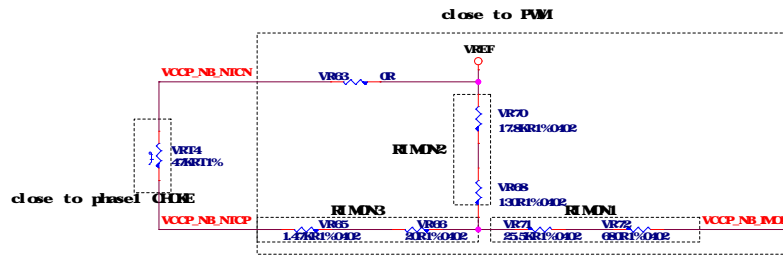
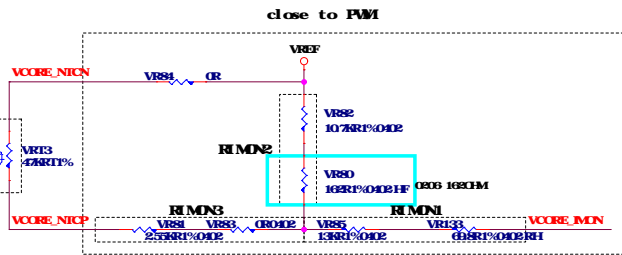
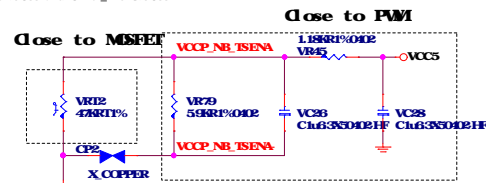
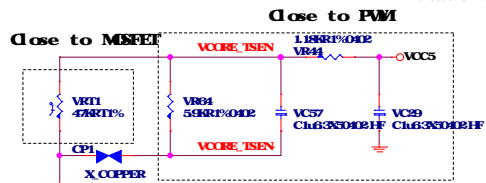
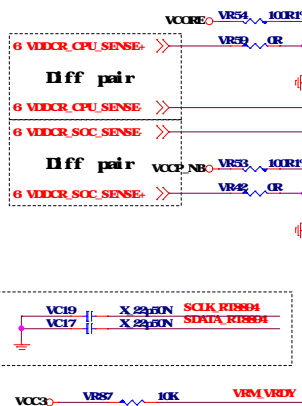
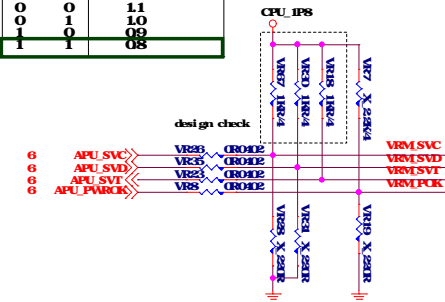


CPU VDDP NOT SUPPORT TYPE2

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RN/ZP	3	1	0

When you use external buffer then you cannot let APU PWR_GOOD pin float in any sleep state. If you're buffer use 3V_S0 and you need Pull-down 100K. If you're buffer use 3V_S5 and you don't need PD.

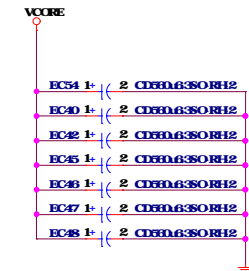
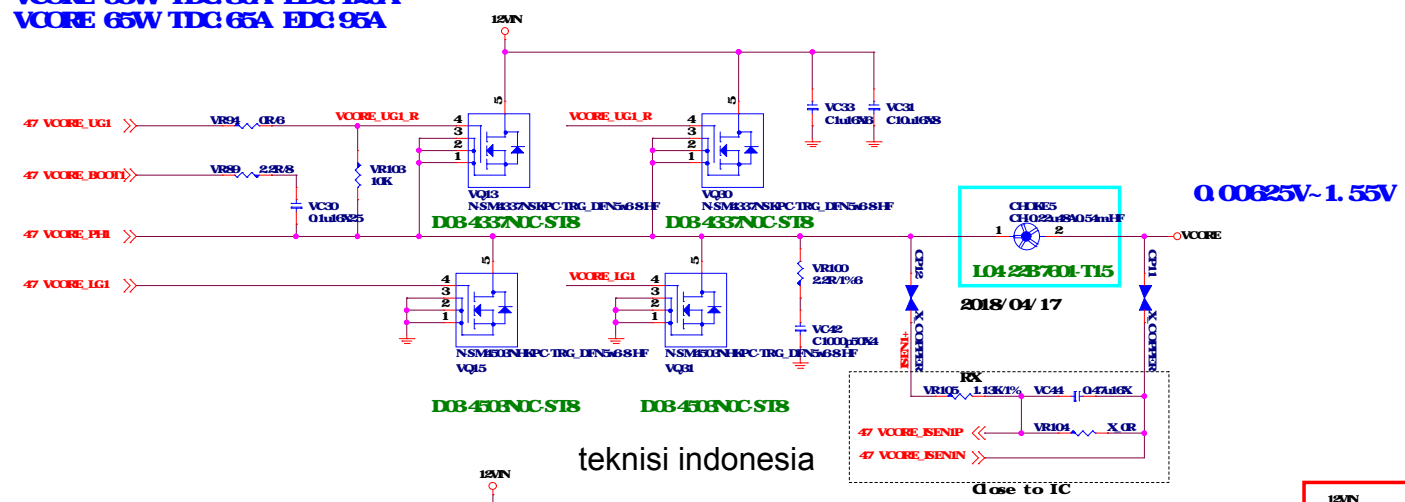
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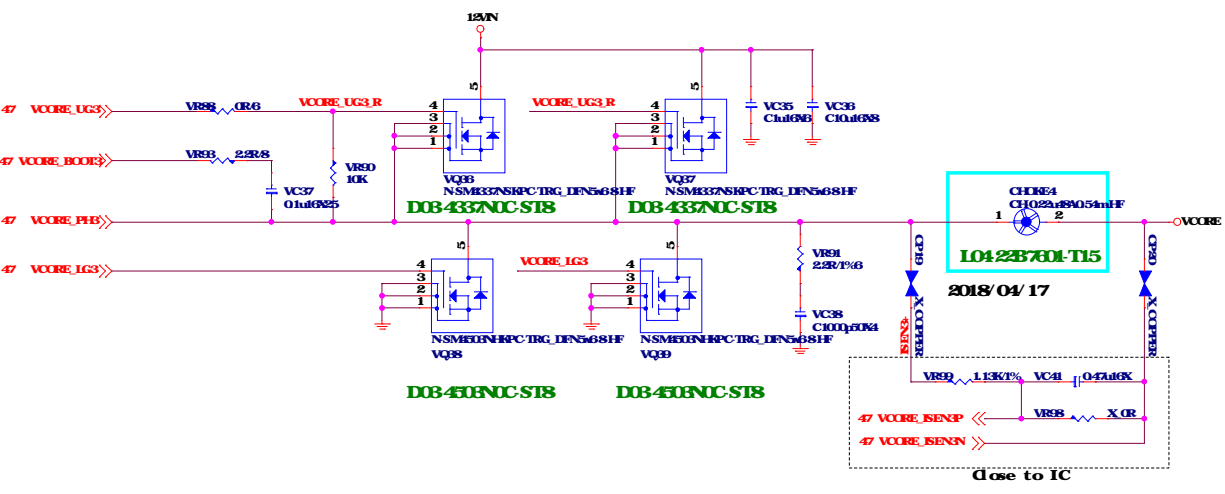
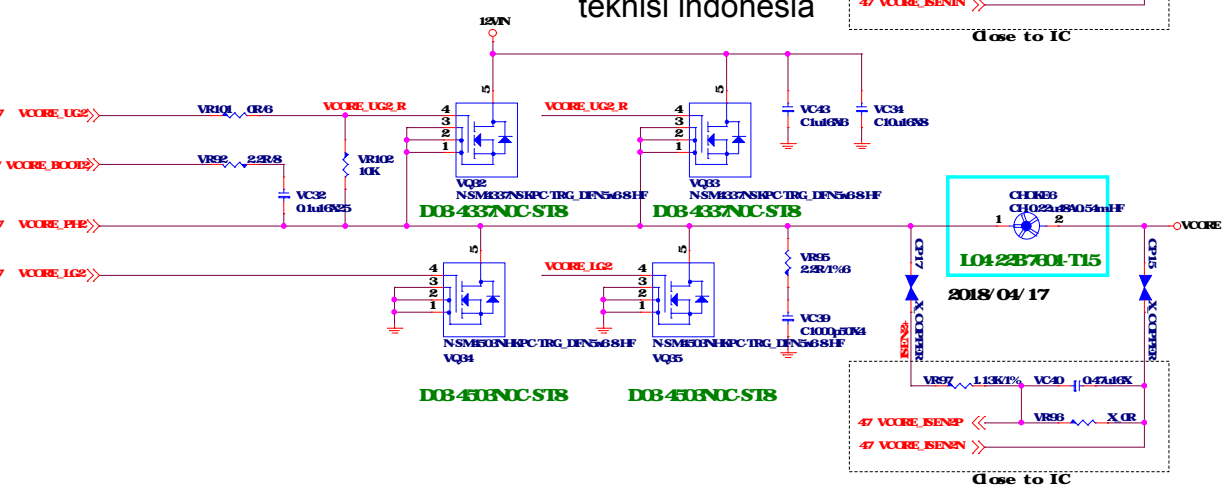
SET1 control	ICOMAX OP setting
SET2 control	Internal compensation

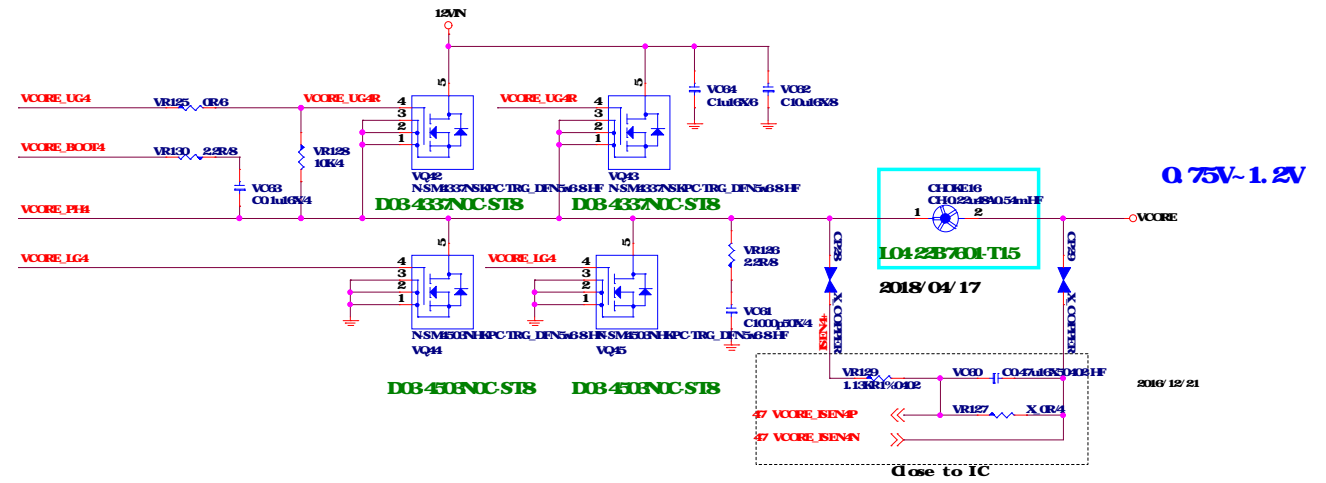
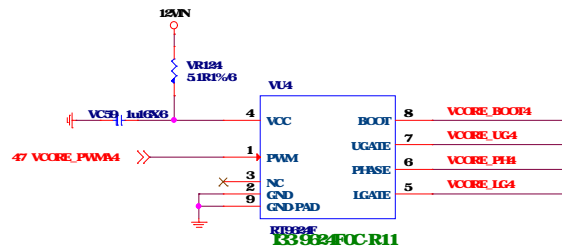
VCCRE IccMAX 125A =>OCP=>200A
VCC_NB IccMAX 75A =>OCP=> 90A

VCORE 95W TDC 80A EDC 125A
VCORE 65W TDC 65A EDC 95A

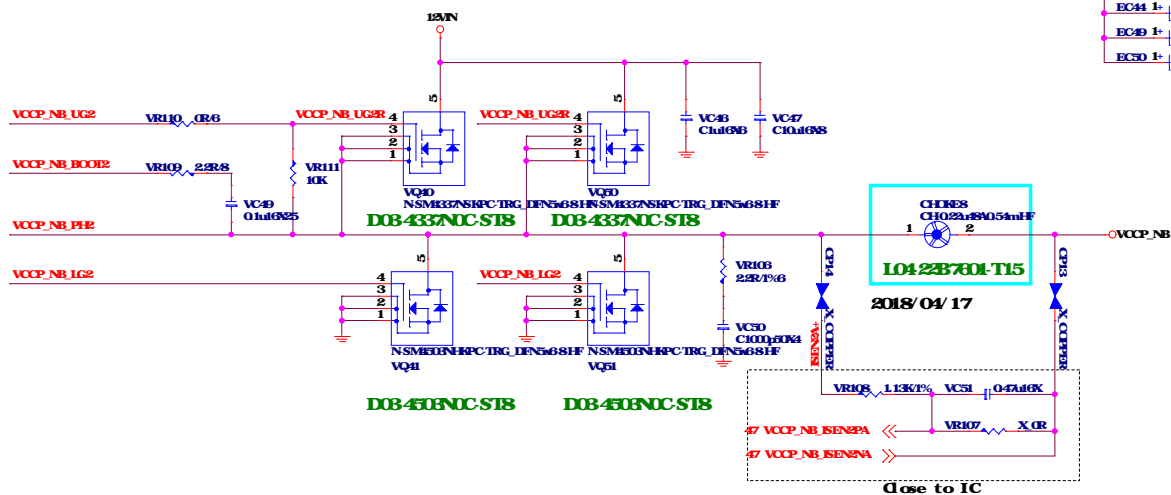
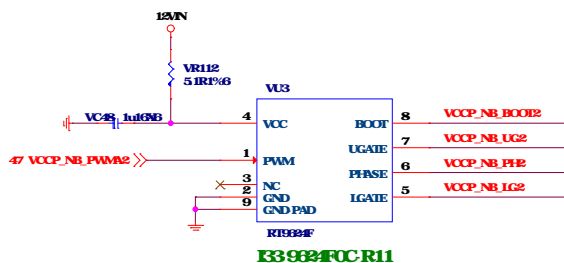
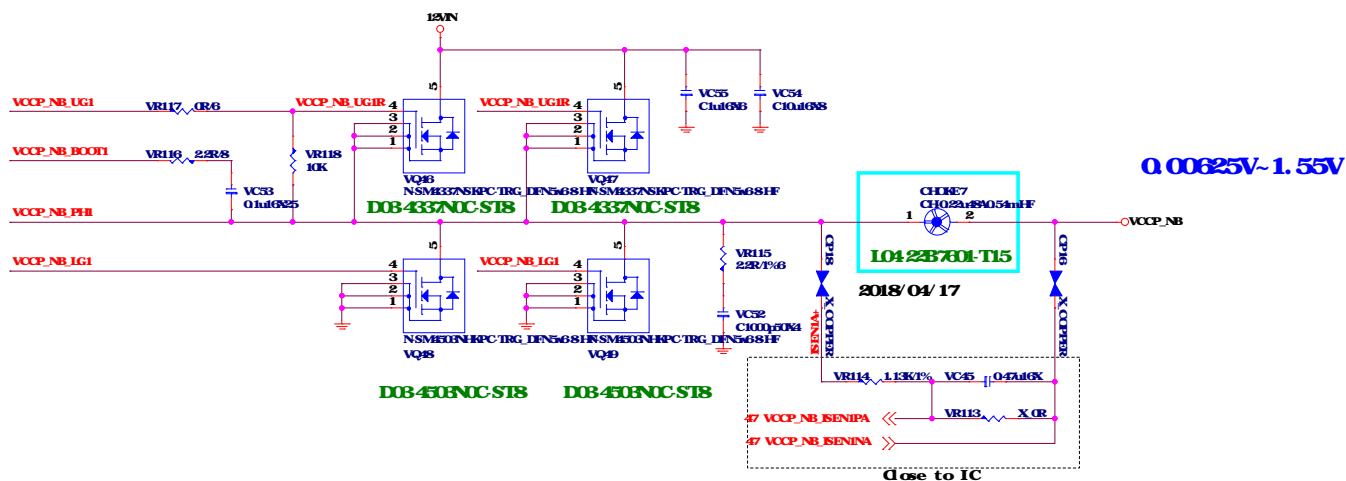
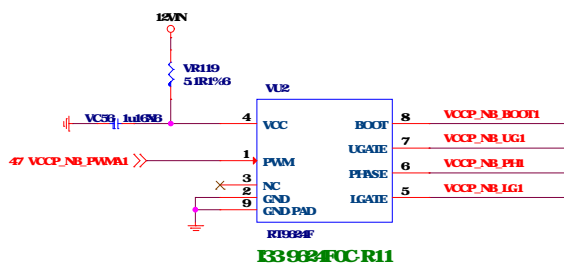


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VCCP_NB 95W TDC 50A EDC 75A
VCCP_NB 65W TDC 50A EDC 75A

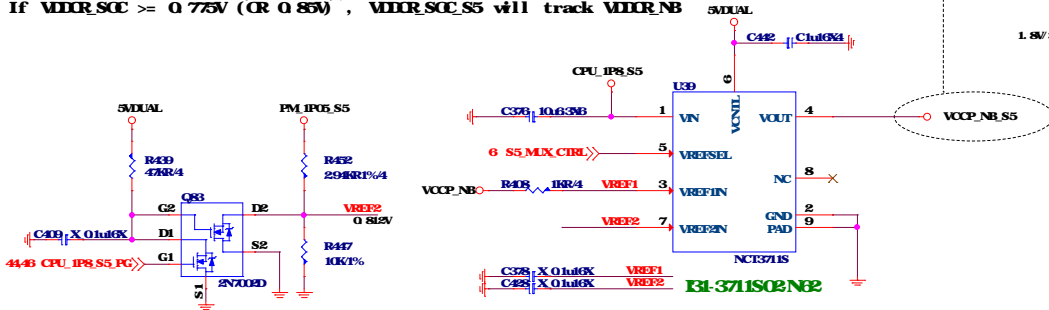


TYPE0 Only

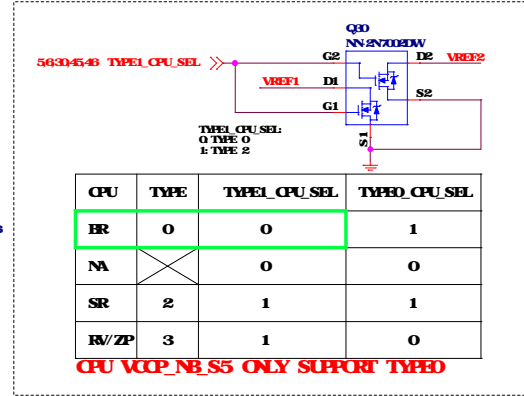
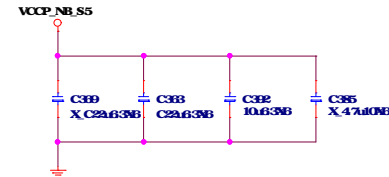
S5_MUX_CTRL
HIGH S0
LOW S3/S5

H +VDDP_FCH_ALW will track VDDNB
L If VDDP_SOC<0.775V (OR 0.85V), VDDP_SOC_S5 =0.775V
If VDDP_SOC >= 0.775V (OR 0.85V), VDDP_SOC_S5 will track VDDP_NB

(VDDP_SOC_S5 is only used for AMD Family 15h Models 60h 6fh processors) Bristol Ridge TYPE0



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CPU	TYPE	TYPE0_CPU_SEL	TYPE0_CPU_SEL
IR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

Over Voltage Control IC

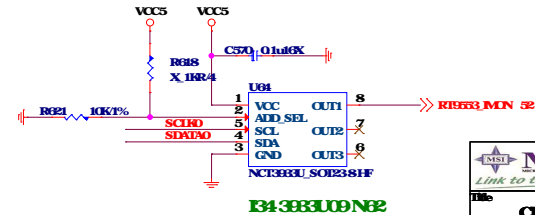
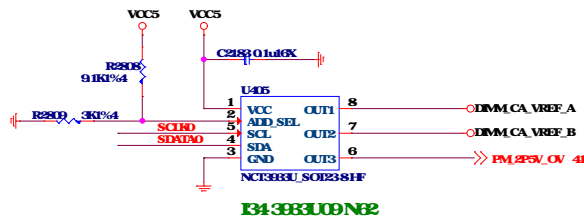
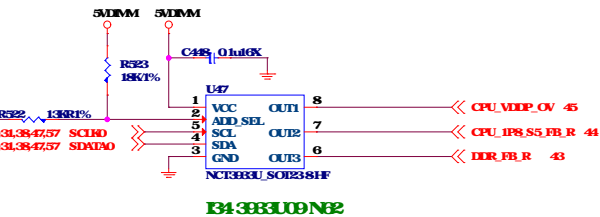
0x20 RH=18K RL=13K

0x28 RH=9.1K RL=3K

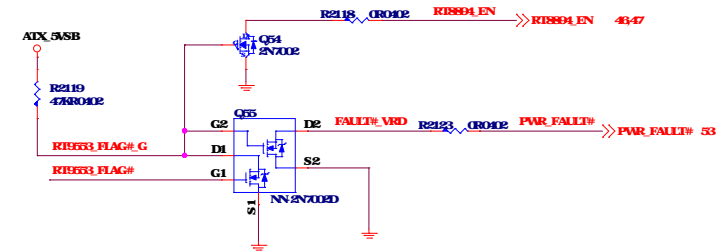
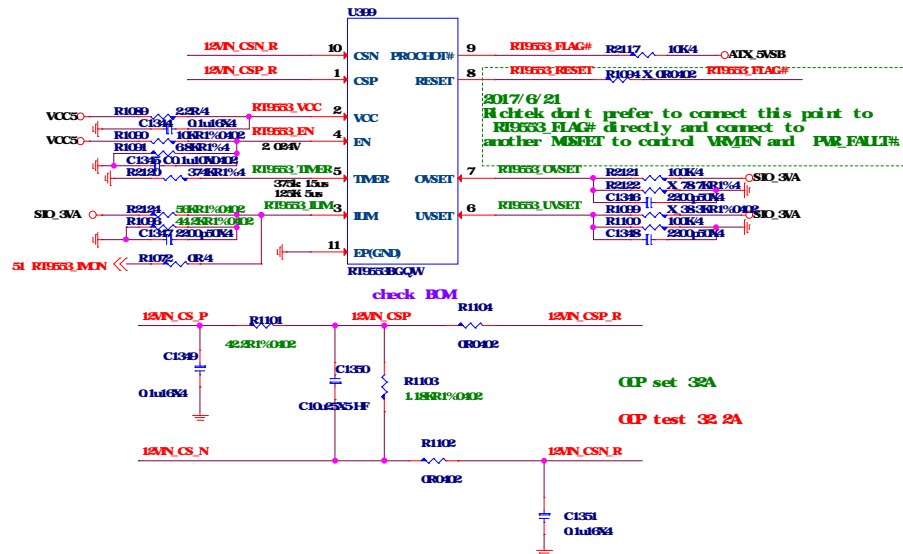
0x2A RH=OPEN RL=10K

UPI VOLTAGE CONTROL

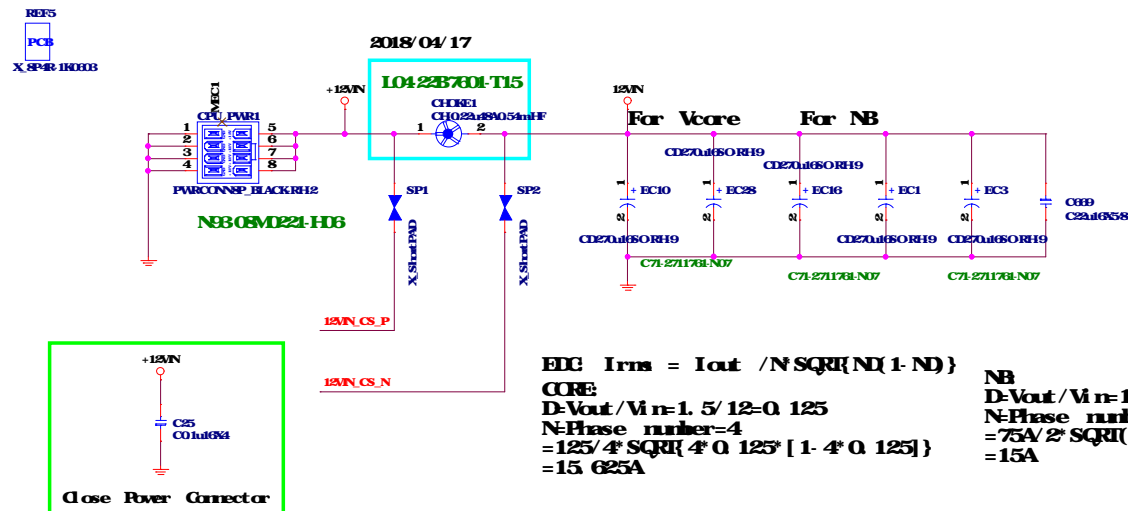
ADDRESS	0x2A	0x28	0x23	0x24	0x22	0x20
RH(40hm)	OPEN	39	3	22	13	10
RL(40hm)	10	13	23	3	39	OPEN
BUS_SEL	0%	23%	40%	60%	73%	100%



VCORE EDC MAC 125A
NB EDC MAX75A



CPU POWER CONNECTOR



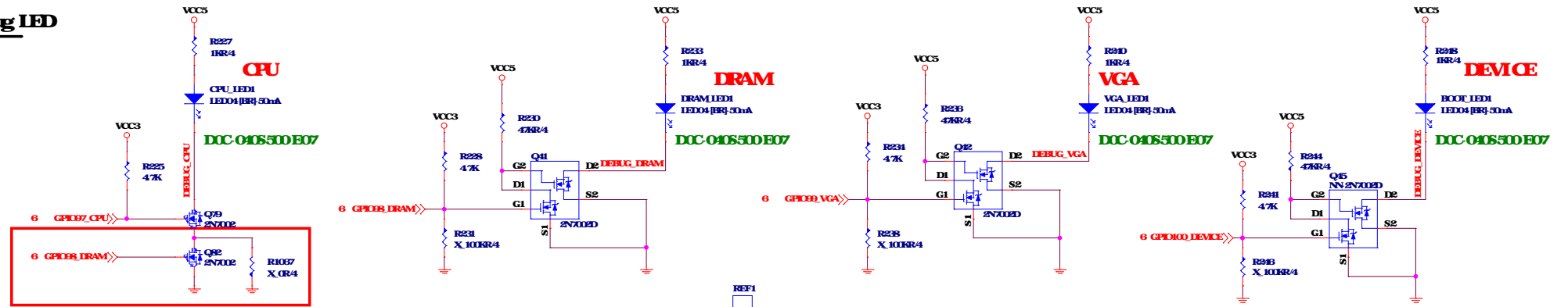
$TDC_{Irms} = I_{out} / N \sqrt{ND(1-ND)}$
CORE:
 $D=V_{out}/V_{in}=1.5/12=0.125$
 $N=$ Phase number=4
 $= 80/4 \sqrt{ND(1-ND)} [1-4 \times 0.125]$
 $= 10A$

NB
 $D = V_{out} / V_{in} = 1.2 / 12 = 0.1$
N-Phase number=2
 $= 654 \cdot 2^{\text{SQRT}(2^0 \cdot 1^* (1 - 2^* 0.1))}$
=13A

EDC Irms = Iout / N*SQR{ND*(1-ND)}
CORE:
D-Vout/Vin=1.5/12=0.125
N-Phase number=4
=125/4*SQR{4*0.125*[1-4*0.125]}
=15.625A

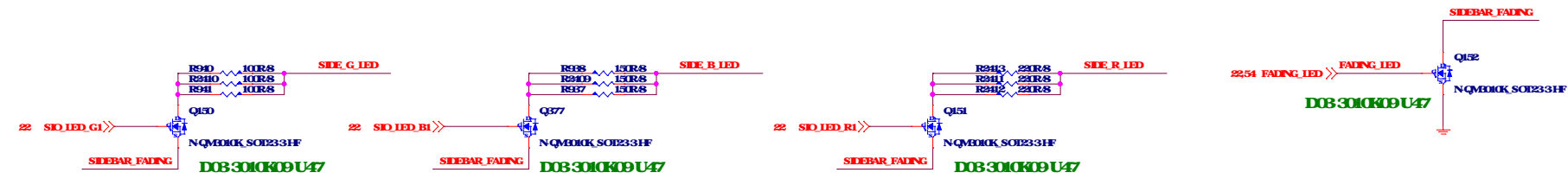
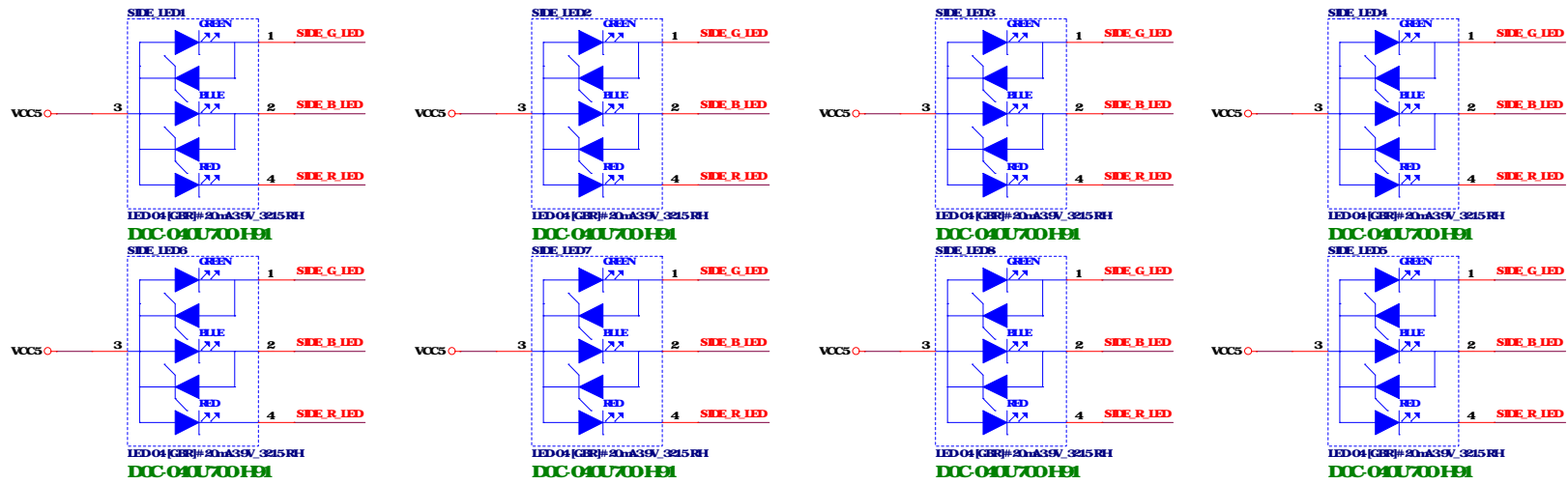
NB
D=Vout / Vin=1.2/12=0.1
N=Phase number=2
=75A/2*SQRT(2*0.1*(1-2*0.1))
=15A

EZ Debug LED

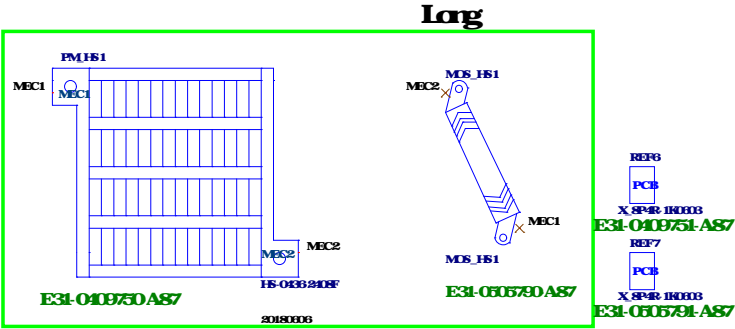


GPIO	GPIO7	GPIO8	GPIO9	GPIO10
LED	GPIO7	GPIO8	GPIO9	GPIO10
	GPIO7	GPIO8	GPIO9	GPIO10
	GPIO7	GPIO8	GPIO9	GPIO10

BOARD SIDE LED



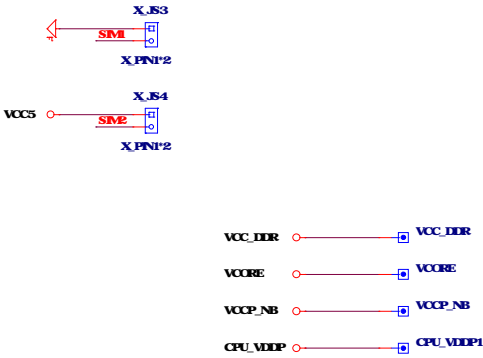
HEAT SINK



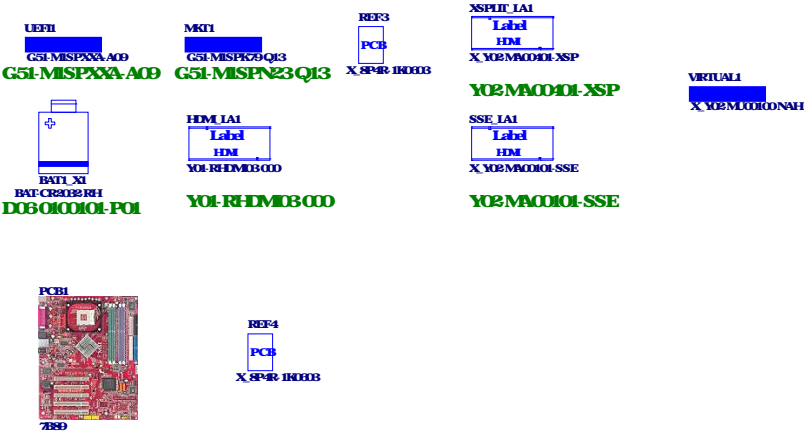
CPU Socket



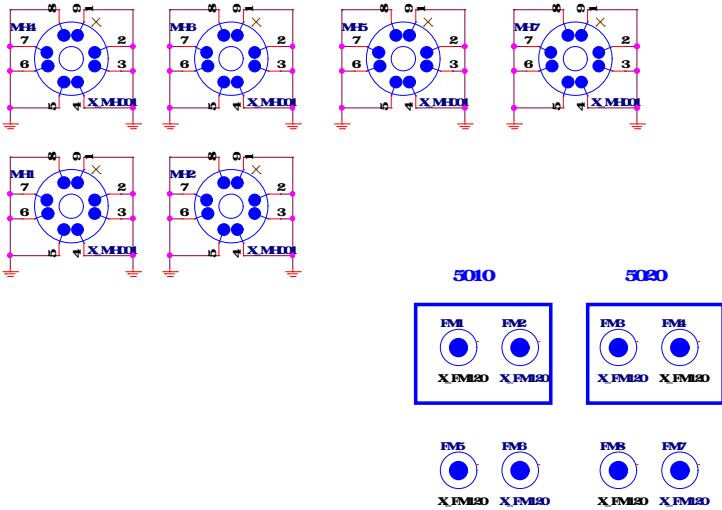
Simulation



MANUAL PART



Optics Orientation Holes



OPT	Configure	BOM	Function
		601- 7A37- A01	XXXX

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File: BOMOption

Site: Custom

Docum: MS-7880

Date: Wednesday, July 04, 2018

Sheet: 53 of 68

Rev: 11

